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# Modeling and implementing a digitally embedded maximum power point tracking algorithm and a series-loaded resonant DC-DC converter to integrate a photovoltaic array with a micro-grid

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# NAVAL POSTGRADUATE SCHOOL

**MONTEREY, CALIFORNIA**

# THESIS

**MODELING AND IMPLEMENTING A DIGITALLY EMBEDDED MAXIMUM POWER POINT TRACKING ALGORITHM AND A SERIES-LOADED RESONANT DC-DC CONVERTER TO INTEGRATE A PHOTOVOLTAIC ARRAY WITH A MICRO-GRID**

by

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September 2014

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# MODELING AND IMPLEMENTING A DIGITALLY EMBEDDED MAXIMUM POWER POINT TRACKING ALGORITHM AND A SERIES-LOADED RESONANT DC-DC CONVERTER TO INTEGRATE A PHOTOVOLTAIC ARRAY WITH A MICRO-GRID

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# ABSTRACT

A DC-DC converter with an embedded digital maximum power point tracking (MPPT) algorithm for a photovoltaic (PV) application is presented in this thesis. The topology centers around a series-loaded resonant (SLR) converter using galvanic isolation that interfaces a PV array with a storage battery connected to the DC bus of an existing micro-grid.

The SLR converter operates in discontinuous conduction mode to minimize the switching losses and for the linear relationship between switching frequency and converter output current. This feature allows for multiple SLR converters to be paralleled, improving the overall efficiency of a PV system by eliminating a central converter and instituting the concept of multiple micro-converters.

The perturb and observe MPPT algorithm employed uses a single voltage sensor and schedules a switching frequency based on the PV array power feedback. The performance of the MPPT algorithm is compared to a similar algorithm that uses both a current and voltage sensor.

In this thesis, the SLR converter control system was simulated, designed, and implemented in the laboratory. The experimental measurements show that the SLR converter presented is an ideal topology for a PV application.

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# LIST OF ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| AC | alternating current |
| CCM | continuous conduction mode |
| DC | direct current |
| DCM | discontinuous conduction mode |
| DIP | dual-inline packaging |
| DON | Department of the Navy |
| FPGA | field programmable gate array |
| G | cell irradiance |
| IC | integrated circuit |
| LC tank | inductor-capacitor tank |
| LUT | look-up table |
| MOSFET | metal oxide semiconductor field-effect transistor |
| MPPT | maximum power point tracking |
| P&O | perturb and observe |
| PCB | printed circuit board |
| PV | photovoltaic |
| ROM | read only memory |
| SLR | series-loaded resonant |
| VHDL | VHSIC hardware description language |
| VHSIC | very high speed integrated circuit |
| ZCS | zero current switching |
| ZVS | zero voltage switching |

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# EXECUTIVE SUMMARY

In 2012, the Department of the Navy (DON) established a goal that by 2020, a minimum of 50 percent of the energy consumed ashore must be provided by a renewable energy source [1]. These renewable energy sources can include solar, wind, geothermal, biomass, hydroelectric, and nuclear. Of these sources, photovoltaic (PV) arrays interfaced directly to the AC grid are increasingly more popular because of the lower initial investment, lower operating cost, and ease of installation; however, the low power density and intermittent nature of solar energy prevent the solar energy industry from unseating fossil fuel energy sources (i.e., coal, oil, and natural gas) as the primary sources of energy. The latter of these problems is being addressed through the use of energy storage systems [2], [3]. The integration of energy storage is vital in making solar energy competitive with fossil fuel energy sources.

The focus of this thesis is a PV power conditioning system feeding storage batteries connected to the DC bus of a micro-grid. This type of system is used to harvest and store solar energy for later usage or to power DC loads, adding both reliability and security to an existing micro-grid. The research presented in this thesis proves that the series-loaded resonant (SLR) converter with galvanic isolation presented in Figure 1 is an attractive topology for PV applications. This topology utilizes a digitally embedded maximum power point tracking (MPPT) algorithm to optimize the output power of a PV array connected to storage batteries on the DC bus of an existing micro-grid.

The objectives of this thesis were to design and build an SLR converter for a PV application and then design and simulate the MPPT algorithm and converter control logic in software. With a functioning SLR converter, MPPT algorithm, and converter control logic, the PV array power conditioning system is then tested using PV arrays placed in the environment.

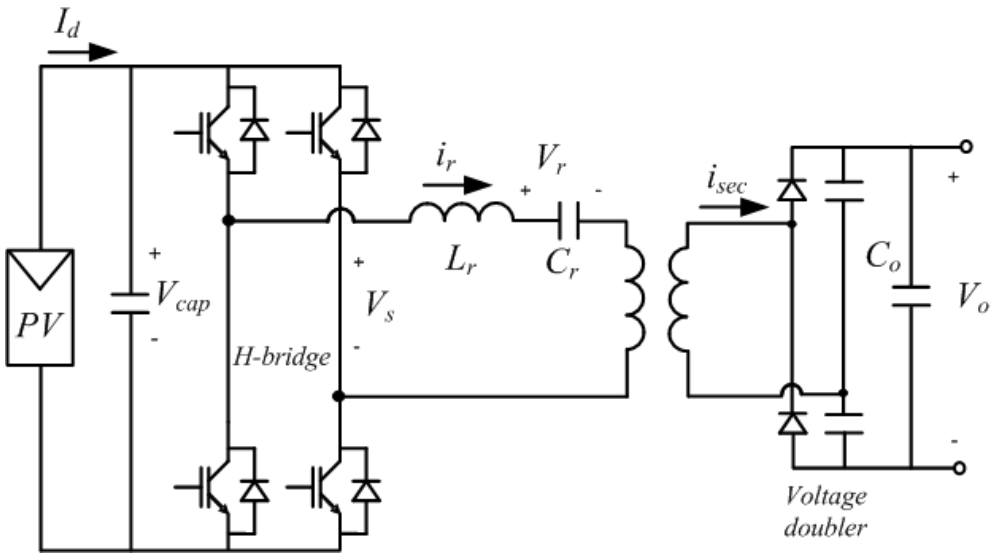


Figure 1. Schematic of a DC-DC SLR resonant converter with galvanic isolation and a voltage doubler.

The final test of the SLR converters was conducted using two parallel 40-W PV arrays connected to the input of the SLR converter. The PV arrays were set up outside and subjected to the varying environmental conditions in Monterey, California. The outputs of the SLR converters were connected in parallel to show the effectiveness of multiple SLR converters operating in parallel.

The output power of the PV arrays and the scheduled switching frequency of the SLR converters were recorded in 21 second intervals. During each 21 second interval, the PV arrays were manipulated to show the response of the MPPT algorithm to varying environmental conditions. The MPPT algorithm response to a slow increase in PV array irradiance can be seen in Figure 2. As the PV irradiance is increased, the maximum power point of the PV array also increases. The MPPT algorithm forces the PV array to operate at the maximum power point by increasing the switching frequency, which, in turn, increases the PV array output current. The increase in PV array output current causes the output voltage to sag based on the non-linear operating characteristics of a PV array. These observations of the PV array output response to the increase in irradiance demonstrate that the MPPT algorithm is operating properly.

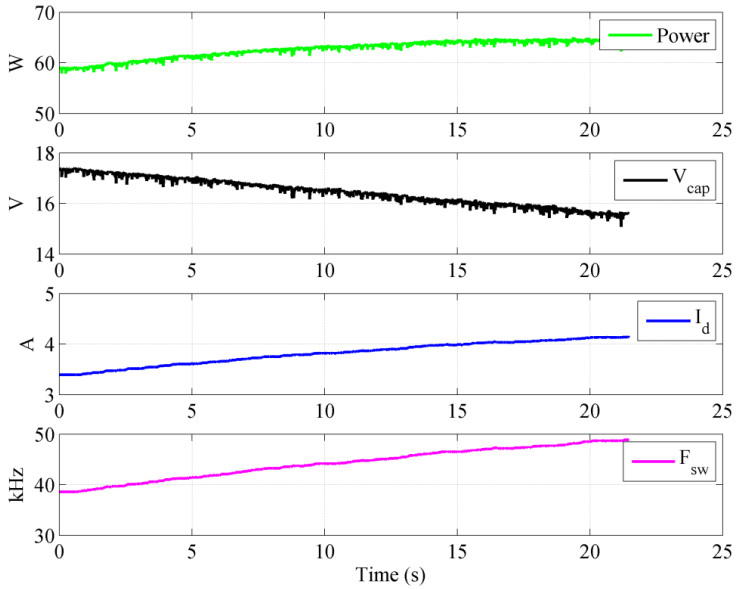


Figure 2. SLR converter waveforms based on a slow increase in PV array irradiance.

In conclusion, the research presented in this thesis demonstrates that the SLR converter topology presented as Figure 1 is an attractive DC-DC converter for PV applications. The features associated with the SLR converter maximize efficiency and allow for multiple converters to operate in parallel. The digitally embedded MPPT algorithm further improves the efficiency of the PV power conditioning system by forcing the PV array to operate at the maximum power point.

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[3] D. V. de la Fuente, C. L. Trujillo Rodriguez, G. Barcera, E. Figueres, and R. O. Gonzalez, “Photovoltaic power system with battery backup with grid-connection and islanded operation capabilities,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp.1571–1581, Apr 2013.

# I. INTRODUCTION

In 2012, the Department of the Navy (DON) established a goal that by 2020, a minimum of 50 percent of the energy consumed ashore must be provided by a renewable energy source [1]. These renewable energy sources can include solar, wind, geothermal, biomass, hydroelectric, and nuclear. Of these sources, photovoltaic (PV) arrays interfaced directly to the AC grid have been increasingly more popular because of the lower initial investment, lower operating cost and ease of installation [2]. From 2001 to 2011, the use of PV arrays doubled and by 2050 is expected to account for more than 10 percent of the energy production in the world [3]; however, the low power density and intermittent nature of solar energy prevent the solar energy industry from unseating fossil fuel energy sources (i.e., oil, coal, and natural gas) as the primary sources of energy. The latter of these problems is being addressed through the use of energy storage systems [4], [5]. The integration of energy storage is vital in making solar energy competitive with fossil fuel energy sources.

As solar energy is generally used to interface directly to an AC bus or the grid, there is an increasing interest in a DC interface of PV arrays. In this manner, PV arrays can then be used to charge batteries or to power DC distribution networks, which are presently being investigated for many applications ranging from local residential DC micro-grids to large commercial micro-grids for data centers [6], [7]. The focus of this thesis is a PV power conditioning system feeding storage batteries connected to the DC bus of a micro-grid. This type of system is used to harvest and store solar energy for later usage or to power DC loads adding both reliability and security to an existing micro-grid.

The use of resonant converters to interface PV panels to batteries or a DC bus have been recently investigated in [8], [9], and [10]; although, not all of the topologies reported feature galvanic isolation. The topology analyzed in this thesis is a full bridge front-end, series-loaded resonant (SLR) converter with galvanic isolation and a voltage doubler on the output as shown in Figure 1. In [10], the topology depicted in Figure 1 is referred to as an LLC converter, which is an SLR converter utilizing a high-frequency transformer for galvanic isolation. In [11] and [12], the SLR converter was analyzed for

applications different than PV conditioning and featured a half bridge inverter at the input and no voltage doubler at the output. In [13], the voltage doubler circuit was investigated; however, the input is a half bridge inverter and, furthermore, the mode of operation is continuous conduction mode (CCM). The topology depicted in Figure 1 operated in discontinuous conduction mode (DCM) has not been previously presented for PV interface application.

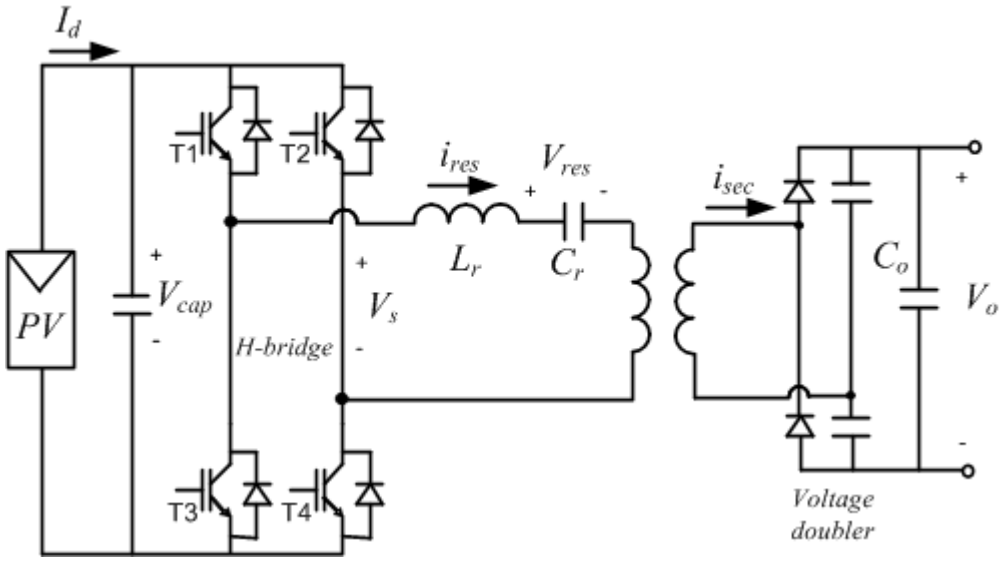


Figure 1. Schematic of DC-DC SLR resonant converter with galvanic isolation and a voltage doubler.

## A. SLR CONVERTER

The SLR converter presented in this thesis was designed and implemented for PV application. The design, operation, and advantages of this topology as they relate to interfacing a PV array to an existing DC micro-grid are detailed in this section.

### 1. Design

The PV power conditioning system includes a DC-DC SLR converter topology with galvanic isolation and a voltage doubler as shown in Figure 1. This topology utilizes a full-bridge front-end with an LC resonant tank in series with the load. The full-bridge front-end ensures that the entire source voltage vice half is applied across each switch as

observed in [8], [9], and [10]. The resonant tank produces two oscillating resonant voltage and current pulses per cycle. The amplitude of the resonant voltage is based on the DC input voltage, while the amplitude of the resonant current is based on both the DC input voltage and the resonant impedance $Z_0$ of the LC tank.

Since the output voltage of the solar panel is relatively low (~ 14 V), there is a pressing need to boost the output voltage to a voltage sufficient enough to charge a 72 V lead-acid storage battery pack. This voltage step-up was accomplished through the use of both a voltage level-shifting high-frequency transformer and a voltage doubler on the output. The voltage level-shifting transformer is a common hand-wound ferrite core transformer.

The voltage doubler utilizes two capacitors in series that charge based on the half-cycle waveform of the resonant tank. Because the two capacitors are in series, the output voltage is the sum of the two capacitor voltages and is ideally twice the input voltage. The use of the voltage doubler reduces the number of turns required on the transformer, whose main purpose is galvanic isolation.

## 2. Modes of Operation

The SLR converter has three available modes of operation and are characterized by the ratio of the switching frequency $f_{sw}$ and resonant frequency $f_{res}$ as given by

$$F = \frac{f_{sw}}{f_{res}}. \tag{1}$$

The three modes of resonant converter operation are:

- discontinuous conduction mode (DCM), where $F < 0.5$
- continuous conduction mode (CCM-1), where $0.5 < F < 1.0$
- continuous conduction mode (CCM-2), where $F > 1.0$

From Figure 2, it can be seen that for values of $F$ less than 0.50, the relationship between the output current and $F$ is nearly linear. This indicates that the output current $I_o$ varies only with switching frequency and is independent of the output voltage $V_o$, which varies with load resistance.

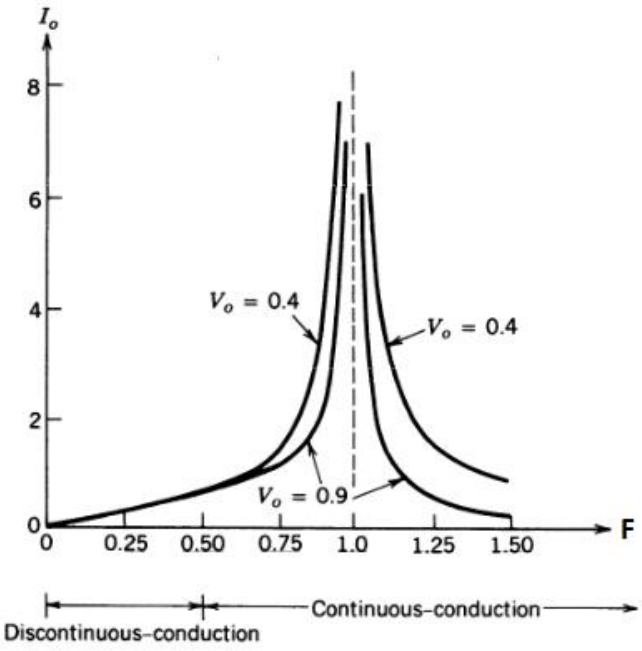


Figure 2. Output current $I_o$ vs $F$ relationship for a series-loaded resonant converter, after [14].

The average output current $I_{out\_avg}$

$$I_{out\_avg} = \frac{1}{T_{sw}} \int |i_{res}(t)| dt = \frac{8 V_s f_{res}}{\omega_o{}^2 L_r} \tag{2}$$

is proportional to the switching frequency, which makes the SLR converter behave like a controllable current source with inherent overload protection while operating in DCM.

In (2) $V_s$ is the H bridge voltage ($V_{cap}$ in Figue 1), $V_o$ is the output voltage, $L_r$ is the resonant inductor and $i_{res}$ is the current in the resonant circuit. All variables are marked in the circuits of Figure 1. The analytical expression for the resonant current $i_{res}$ and the derivation of (2) can be found in [11].

### 3. Switching Losses

Power converters can be grouped in one of two groups, hard switching or soft switching, depending on the way the power switches are turned on and off. The switching and conduction losses in a typical hard switching converter are shown in Figure 3.

In this research, the switch type used is a metal oxide semiconductor field-effect transistor (MOSFET), which utilizes a gate signal to turn the switch on and off. When a 5 V signal is applied to the gate of the MOSFET, the switch turns on, and when no voltage is applied to the gate, the MOSFET turns off. From Figure 3, the voltage and current transients $V_T$ and $I_T$, respectively, for a typical hard switching event are shown, where the MOSFET is initially on and under load before being turned off.

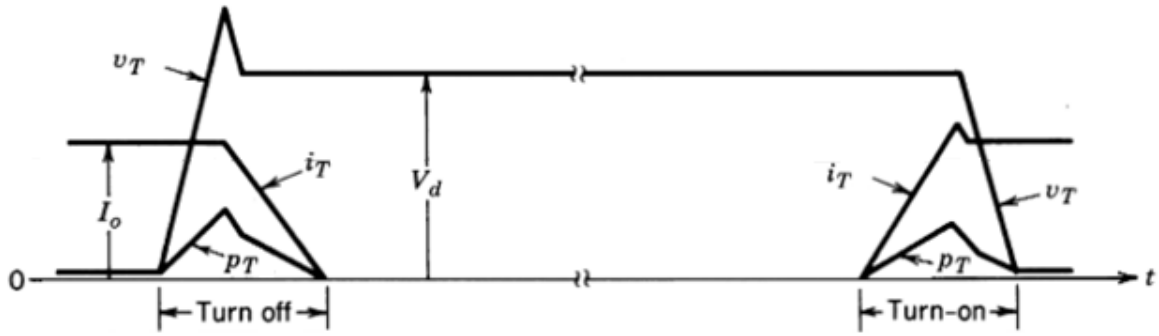


Figure 3. Diagram of voltage and current during a switching event, after [14].

When the gate signal to the MOSFET is removed, the current continues to flow through the MOSFET until the voltage across the MOSFET increases to a value that is the sum of the steady-state voltage of the system $V_d$ and the forward bias voltage of the diode; therefore, a finite period elapses where neither voltage nor current are zero during the on-to-off transition. The product of the non-zero voltage and current is a switching event power loss $P_T$. Once the MOSFET is off and the voltage across the switch is greater than the forward bias voltage of the diode, the current through the MOSFET drops to zero, and the power loss decreases to zero. During the MOSFET turn-on, a gate signal is applied, and the current through the MOSFET must increase to the steady-state value for the system $I_o$ plus the reverse recovery current of the diode before the voltage across the MOSFET decreases to zero. As observed with the on-to-off switching event, a finite period occurs where both voltage and current are present during the off-to-on transition and switching power loss occurs. The final power loss associated with switching power supplies is the conduction loss observed while the MOSFET is on. As shown in Figure 3, with a gate signal applied to the MOSFET operating in steady-state, the voltage across

the MOSFET is not zero; there is a small voltage drop across the MOSFET based on the drain-to-source resistance value $R_{ds}$ of the MOSFET utilized in the circuit.

The SLR converter presented in this thesis is a soft switching converter, where the switching losses are eliminated because the switching events occur when either the voltage or current are equal to zero as shown in Figure 4.

For all modes of operation, switches T1 and T4 and T2 and T3 (as shown in Figure 1) operate as pairs. Furthermore, while T1 and T4 are on, T2 and T3 must be off to prevent applying a short across the input power source. In Figure 4, T+ represents the period when switch pair T1 and T4 is on, and T- represents the period when switch pair T2 and T3 is on. During the D+ period, diode pairs D1 and D4 conduct while switches T1 and T4 are off, and during the D- period, D2 and D3 conduct while switches T2 and T3 are off. Note that in Figure 1 the diodes D1 through D4 are the diodes in antiparallel with the devices T1 through T4, respectively.

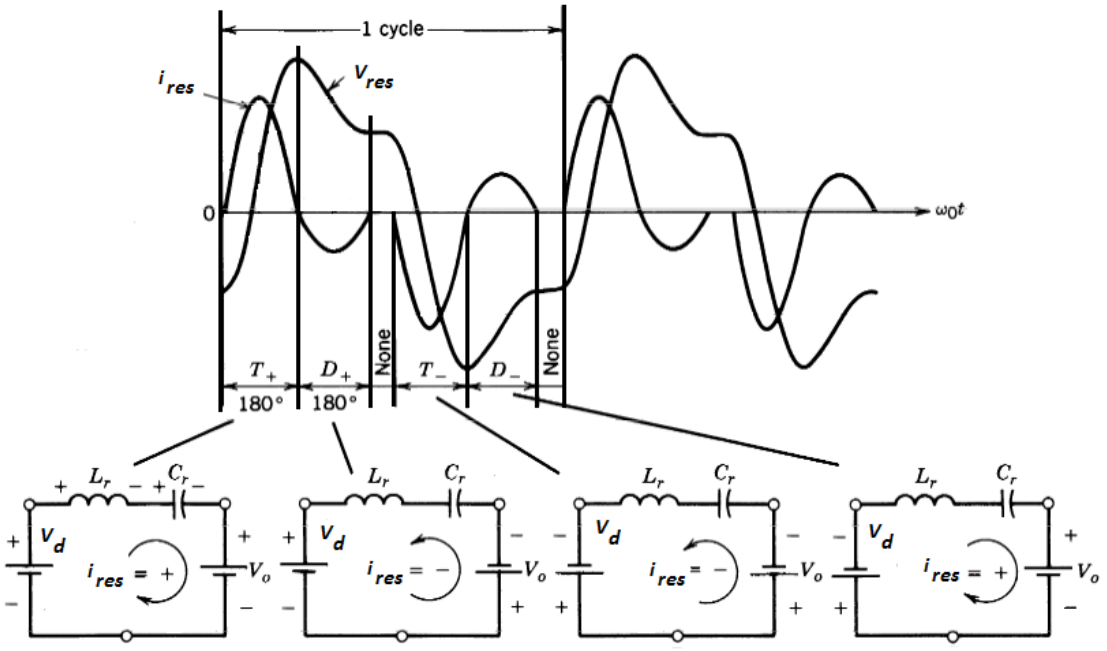


Figure 4. Voltage and current waveforms while operating in DCM, after [14].

## 4. Advantages

An advantage of the SLR converter operating in DCM is that the output current is linearly proportional to the switching frequency, providing excellent power flow control. This linear characteristic makes the SLR converter behave as an ideal current source and allows for paralleling multiple converters to support higher power applications. Each converter can have variations in its operation based on component manufacturing tolerances, but this has no ill-effects on the system because each converter is operating as a DC current source where the output currents of the paralleled converters are algebraically summed and distributed to the DC bus of a micro-grid.

The soft-switching feature that is inherent to operation in DCM is an additional advantage to this topology. The SLR converter output power can be controlled by changing the switching frequency while not affecting the switching losses, in the converter. The soft-switching minimizes the switching losses, providing a nearly constant efficiency over a varying range of input voltages. Zero current switching (ZCS) is also observed during operation of the SLR converter. This is observed when each output rectifier diode stops conducting before the other turns on.

With the fine control of power flow and the enhanced efficiency of an SLR converter compared to a typical boost converter, this topology is an attractive interface for PV arrays. The recent trend to replace large centralized converters with small converters (sometimes called micro-converters [15]) that interface single PV cells is based on the need to reduce the negative effects of shading and manufacturing differences between panels. Furthermore, MPPT algorithms are more effective when applied to individual PV cells vice large PV arrays. There are some drawbacks to the use of micro-inverters such as the increased cost; however, as the cost of semiconductors continues to decrease and micro-inverters are shown to increase the overall efficiency of the PV array, centralized converters will become obsolete.

For these reasons, only the application of the series-loaded resonant converter operating in DCM is examined in this thesis.

## B. MAXIMUM POWER POINT TRACKING

The SLR converter utilizes an MPPT algorithm that is digitally embedded in the controller logic. The MPPT algorithm has been shown to increase the overall efficiency of a PV array by ensuring that the output power is always optimized for the current environmental conditions. The purpose of a MPPT algorithm and the MPPT method chosen to be implemented in this thesis are detailed in the following sections.

### 1. Purpose

The output characteristics of a PV array are non-linear (see Figure 5). The PV array current does not vary linearly as voltage varies. These non-linear characteristics are based on the design of the PV cell as well as the environmental conditions in which the cell is operating. To force the PV array to operate at the maximum power point, a MPPT control algorithm coupled with switching power converter must be utilized. The MPPT control algorithm dictates the power converter switching scheme and varies the load impedance as observed by the PV array. The concept of varying the load impedance of a PV array is only applicable if the PV array is not powering a fixed load but instead connected to a storage battery in parallel with a load or tied to an existing grid utilizing either commercial power or another distributed generation resource.

Because the PV array in this thesis is charging a lead-acid storage battery connected to a DC micro-grid, the output of the PV array is not affected by the load impedance of the micro-grid. This means that the output of the PV array, and thus, the output of the SLR converter can vary without affecting operation of any peripheral load connected to the micro-grid so long as the storage battery has a sufficient charge or an additional source of power is available. This is also true if the output of the PV array is connected to an AC grid via a DC-AC converter since there are no loads dependent upon the voltage or current being supplied by the PV array alone.

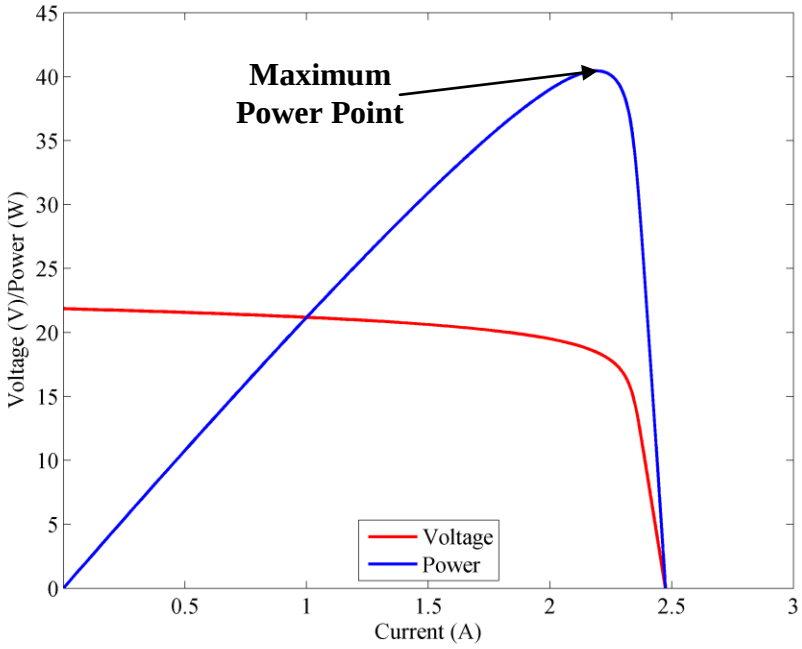


Figure 5. Typical voltage versus current and power versus current profile for a 40-W PV array.

The MPPT algorithm optimizes the output power of the PV array by varying the load impedance seen by the PV array. The algorithm forces the PV array to operate at the maximum power point, or the "knee," of the voltage versus current curve. In this case, the load impedance is provided by the SLR converter via a closed loop controller that schedules the switching frequency based on a desired output power.

## 2. Methods

There are multiple MPPT methods that are in use currently [16]. These range from complex algorithms that use neural networks and fuzzy logic to simple algorithms that utilize the general principles of calculus. The method employed in this thesis is of the later variant and is commonly known as either the perturb and observe (P&O) or hill-climbing method. This method exploits a fundamental of calculus; specifically, that the derivative at the local maximum of a curve is equal to zero. Thus, the derivative on the left side of the local maximum is greater than zero, and the derivative on the right side of the local maximum is less than zero.

There are multiple versions of the P&O algorithm including both the fixed step and variable step methods [17]; however, the focus of this thesis is on the fixed step method where $I_d$ is incremented or decremented by a fixed value. A simplified block diagram of the P&O MPPT algorithm is shown in Figure 6 and described in the next section.

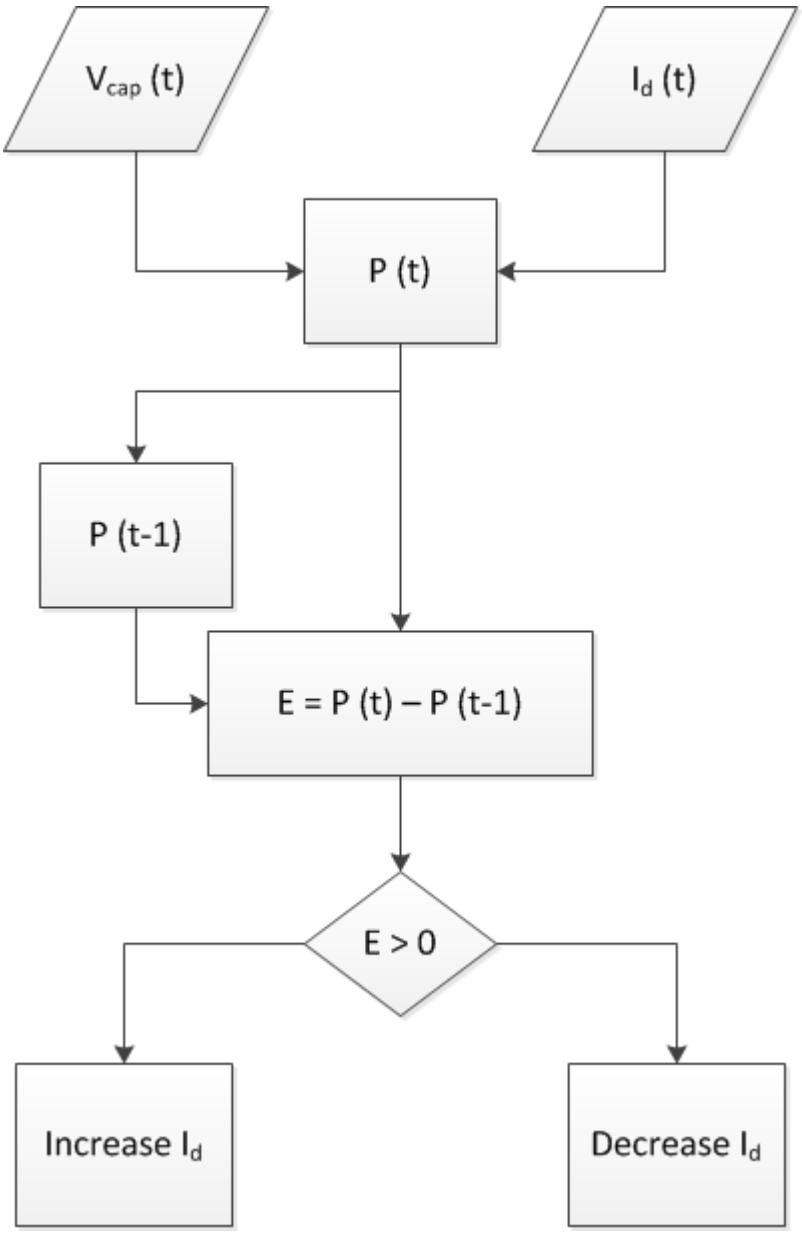


Figure 6. Simplified block diagram of P&O MPPT algorithm.

## 3. Operation

The P&O algorithm requires two inputs, PV array output current $I_d$ and voltage $V_{cap}$, to find the operating point that yields the maximum power output of the PV array. The P&O algorithm calculates the power of the PV array by multiplying the output current and voltage. Because the P&O MPPT method focuses on the polarity of the derivative combined with using a fixed sampling rate, the only operation of concern is the difference between the current and previous output power. Dividing this difference by a small fixed sample period does not affect the polarity of the result and is neglected. An error signal $E$ is produced by taking the difference between the current output power $P(t)$ and the output power calculated from the previous sample $P(t–1)$. Based on the polarity of $E$, the MPPT algorithm either incrementally increases or decreases the PV array output current. For example, if the error signal is positive, indicating that the PV operating point is to the left of the maximum power point, $I_d$ is incremented by a fixed step $\Delta I$ until the polarity of the error becomes negative. Of note, the PV array output voltage could also be varied to control the PV array output power, but since the SLR converter researched as part of this thesis operates as an ideal current source, the preferred variable is the PV array output current.

A drawback of the P&O algorithm is that the actual maximum power point is never reached; instead the algorithm causes the operating point of the PV array to oscillate around the maximum power point. The amplitude of these oscillations is based on the value of $\Delta I$ that is coded in software.

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# II. INITIAL HARDWARE SET UP AND MEASUREMENTS

In order to properly model the MPPT algorithm, the SLR converter had to be built and tested. The process of designing, building, and testing the SLR converter are detailed in the following section.

## A. HARDWARE DESIGN

With a finalized topology design, the next step was to construct the SLR converter. The process of selecting the appropriate resonant components and the construction of the high-frequency transformer is described in the following section.

### 1. Resonant Component Selection

An SLR converter, as shown in Figure 1, was designed and implemented on a small custom printed circuit board (PCB) as shown in Figure 7. The PCB layout of the SLR converter is also provided in Appendix A. Two identical PCBs were constructed so that during final testing two SLR converters operating in parallel can be tested.

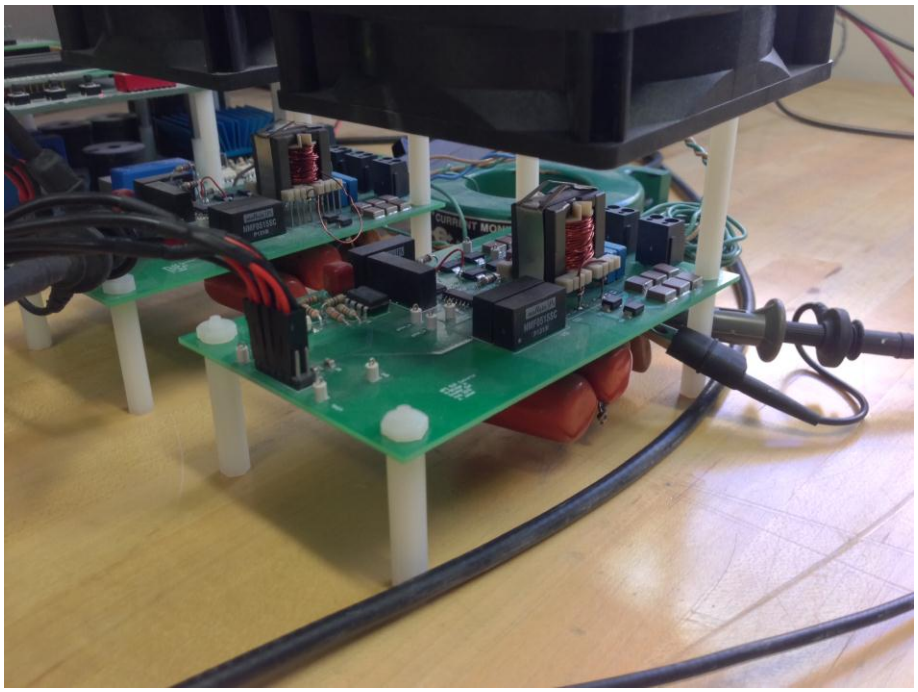

Figure 7. SLR converter with cooling fan.

From AC electrical theory, we get

$$Z_0 = j\omega_0 L_r + \frac{1}{j\omega_0 C_r} \tag{3}$$

as the expression for an LC tank impedance $Z_0$, where $\omega_0$ is the resonant radian frequency, $L_r$ is the resonant inductance and $C_r$ is the resonant capacitance. Based on (3), in order to maximize the power flow through the LC tank, $Z_0$ must be minimized. This was accomplished by designing the converter with a large resonant tank capacitance $C_r$ and minimal resonant inductance $L_r$. There are negative effects associated with minimizing $Z_0$, the primary one being increased conduction losses in the resonant circuit. With lower values of $Z_0$, the resonant pulses get larger. The $Z_0$ must be balanced such that maximum power transfer through the resonant tank is achieved without incurring excessive power loss. To further minimize these conduction losses, the lead lengths between the resonant tank components on the PCB were minimized. The final values of $C_r$ and $L_r$ are included in Table 1.

## 2. Transformer Selection

The output voltage of the PV array was approximately 14 V nominal and required voltage step-up to a voltage greater than 72 V in order to charge the storage battery. With a voltage doubler on the output, the transformer turns ratio $N_t$ necessary to achieve a sufficient output voltage from the SLR converter was determined to be a minimum of 1:3. A margin of safety was added that increased $N_t$ to a minimum of 1:5 such that 72 V could still be achieved if the input voltage were to sag as well as to overcome parasitic losses in the circuit. Two ferrite core transformers were hand-wound in the laboratory where it was observed that based on the diameter of the wire utilized and the size of the transformer cores, the maximum turns ratio that could be achieved was 1:5.5. For the two PCBs used in this experiment, each utilized a transformer with the maximum $N_t$ of 1:5.5; the PCB-1 transformer used 20:110 primary-to-secondary winding, whereas PCB-2 transformer used an $N_t$ of 10:55 to achieve the same step-up in voltage. However, PCB-2 used larger diameter wire than was used in PCB-1. These two transformer designs were done to determine whether the transformer design was a contributing factor in the lower than expected efficiencies. Based on the large resonant current pulses, the small diameter

wiring used for the transformer windings may be causing high conduction losses. By doubling the cross-sectional area of the copper in the windings, the efficiency for PCB-2 will be higher. However as observed during final testing, these transformer differences had no discernable effect on the converter efficiency.

For each transformer design utilized, the primary and secondary currents were measured to ensure the transformer was not operating in the saturation region. Using (4) and the winding ratio discussed above, we observed that neither transformer core was saturating during operation. The expected current step-down ratio was 5.5 to 1, and the observed primary and secondary currents were 11.4 A and 2.1 A, respectively. Using

$$\frac{I_{pri}}{I_{\text{sec}}} = \frac{N_{\text{sec}}}{N_{pri}} \tag{4}$$

and the primary and secondary current values observed, we observed a current step-down ratio of approximately 5.4 to 1 for both transformer designs. The measured primary and secondary currents are plotted in Figure 8 for two different switching frequencies. The gate drive voltages are shown as well, which are discussed in the next section.

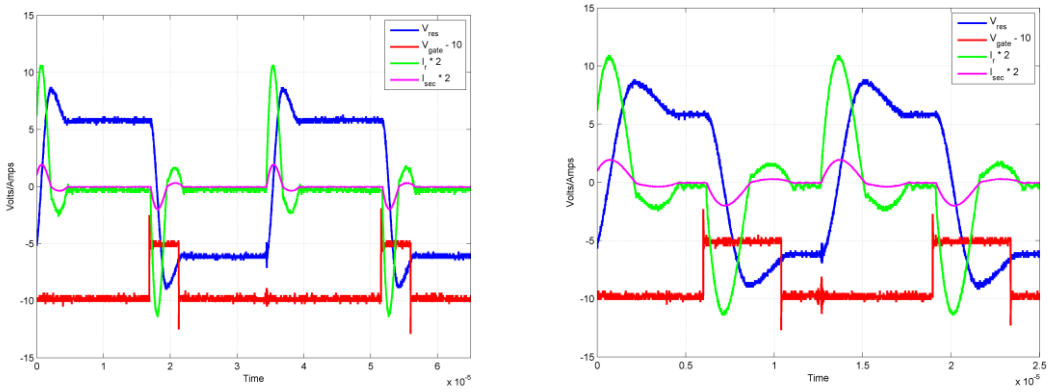


Figure 8. Experimental waveforms at $f_{sw}$ = 46.5 kHz (left) and 94.3 kHz (right): voltage across the resonant capacitor $V_{res}$, gate voltage $V_{gate}$, current on the resonant tank $I_{res}$, and current on the secondary of the transformer $I_{sec}$.

The final circuit parameters are shown in Table 1.

Table 1. Lab experiment parameters

| Parameter | Symbol | Value |
|---|---|---|
| Resonant capacitance | $C_r$ | 0.72 µF |
| Resonant inductance | $L_r$ | 3.1 µH |
| Output capacitor | $C_o$ | 0.2 µF |
| Input voltage | $V_{PV}$ | 14.1 V |
| Transformer turns ratio | $N_t$ | 1:5.5 |
| Output voltage | $V_o$ | 72 V |
| MOSFET Resistance | $R_{ds}$ | 0.02 Ω |

## B. INITIAL HARDWARE SETUP

With the construction of the SLR converters complete, the next step was to connect the converter to the Virtex-4 development board and set the parameters vital to proper operation of the converter. The necessary connections of the SLR converter and the process of setting the pulse-width of the gate voltage to ensure proper operation of the converter are detailed in the following section.

### 1. SLR Converter Connections

For the preliminary testing and data collection, the SLR converter input was a DC power supply that did not mimic the non-linear operation of a PV array but allowed for manual input voltage control. The use of the DC power supply was necessary to collect data to determine the relationship between the switching frequency and output current. Throughout the initial testing of the SLR converter, the output was connected to a separate DC power supply and resistor bank that simulated a lead-acid storage battery. The DC power supply voltage was maintained at 72 V, and a resistor bank was connected in parallel with the DC power supply to dissipate the current from both the DC power supply and the output of the SLR converter. The laboratory setup with the DC power supply and output resistor bank is shown in Figure 9 and Figure 10.

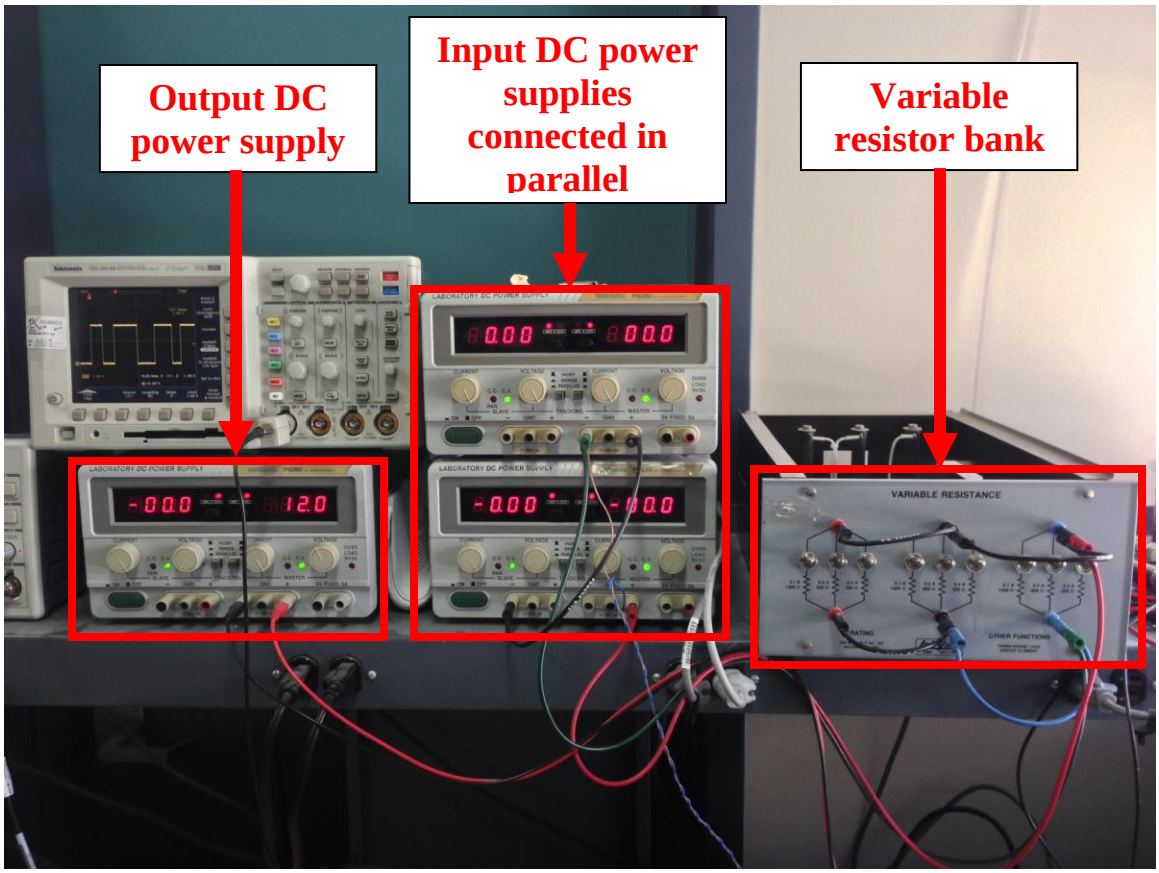


Figure 9. Input and output DC power supplies and output resistor bank.

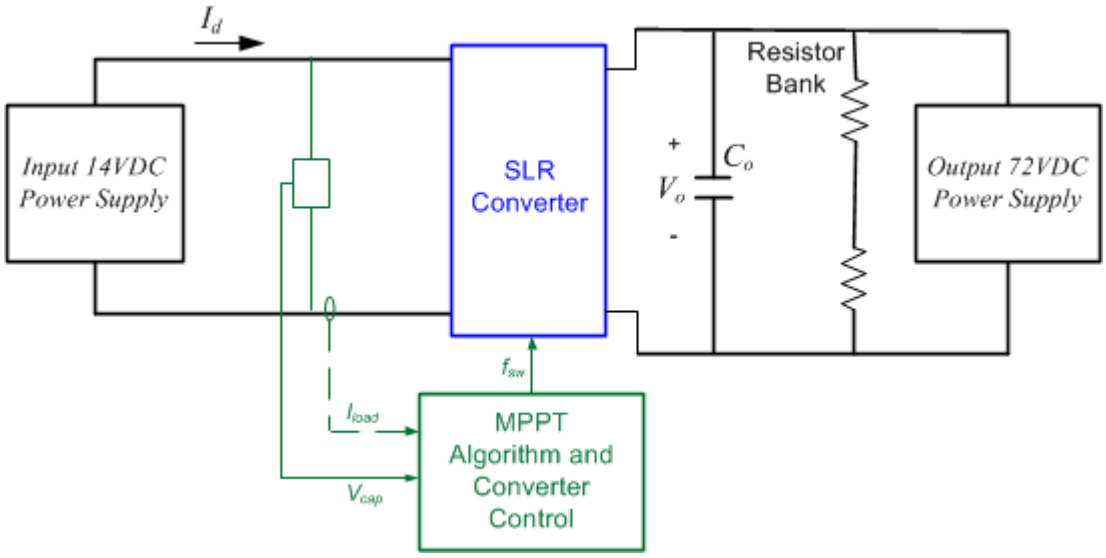


Figure 10. Block diagram of laboratory setup for initial testing.

The SLR converter input current was measured using the built-in ammeter associated with the DC power supply. The output current was determined by taking the difference in current readings on the output DC power supply with the SLR converter on and off. This was necessary because the output DC power supply maintained a constant 72 V and was connected to a resistor bank; therefore, current was supplied by the power supply with the converter both on and off. With the converter on, the DC power supply was supplemented by the output of the SLR converter. In order to determine the output current of the SLR converter, the current output by the DC power supply was recorded with the converter on and off, and the difference was the SLR converter output current. An external connection was placed in series with the LC tank, where a short run of wire was used so that a current probe could be attached to measure the resonant current in the circuit.

Two voltage measurement probes connected to an oscilloscope were used; the first connected across $C_r$ to measure the resonant voltage and the second connected to externally mounted pins to measure the voltage applied to a single pair of MOSFETs.

Additional connections were made between the PCB and the Virtex-4 development board to supply the necessary gate signals to the MOSFETs, to provide a 5 V power supply to the PCB, to provide the voltage feedback as measured on the PCB, and to provide the gate signals to the MOSFETs based on the scheduled switching frequency. The laboratory setup of the Virtex-4 field programmable gate array (FPGA) and the two PCBs is shown in Figure 11.

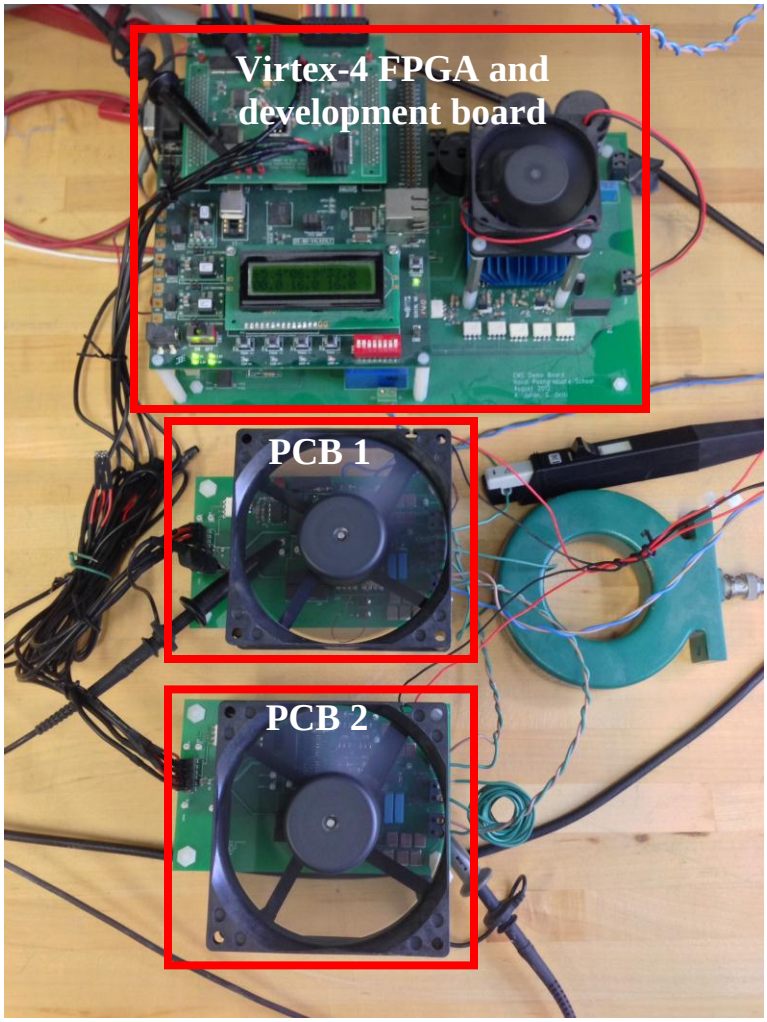


Figure 11. Two SLR converters with cooling fans connected in parallel and the Virtex-4 FPGA and development board.

### 2. Gate Voltage Pulse-width

From Figure 8, the SLR converter waveforms while operating in DCM are shown at two different switching frequencies: 46.5 kHz and 94.3 kHz. The gate voltage is displayed for one pair of MOSFETs, while the resonant voltage and current pulses are shown for both pairs of MOSFETs. The gate voltage pulse length is a parameter set in the digital controller's software and is based on the resonant period. Based on known values of $C_r$ and $L_r$, an initial estimate of the resonant period $T_{res}$ was determined using

$$T_{res} = 2\pi\sqrt{L_r C_r} \ . \tag{5}$$

This resonant period establishes the maximum pulse width of the gate signal that can be applied to a MOSFET to prevent additional pulses from occurring. Through testing, the desired pulse length was determined to be 75 percent of the maximum pulse length. This ensures that gate voltage is removed while the diode is conducting and the voltage across the switch is zero, resulting in soft-switching of the MOSFETs and increasing the efficiency of the SLR converter. From Figure 12, it can be seen that the gate voltage signal remains applied while the switch is conducting to prevent a hard-turn-off event of the converter and is removed about half way through the conduction period of the diode to prevent a subsequent undesired switch turn-on event (i.e., ringing in the resonant tank circuit). It can also be seen in Figure 8 that as the switching frequency increases, the resonant pulses occur more frequently and, therefore, result in a higher average output power.

With the SLR converter gate pulse length established, initial testing was conducted to tune the voltage-to-frequency converter and to determine the gain and offset between the switching frequency and converter output current.

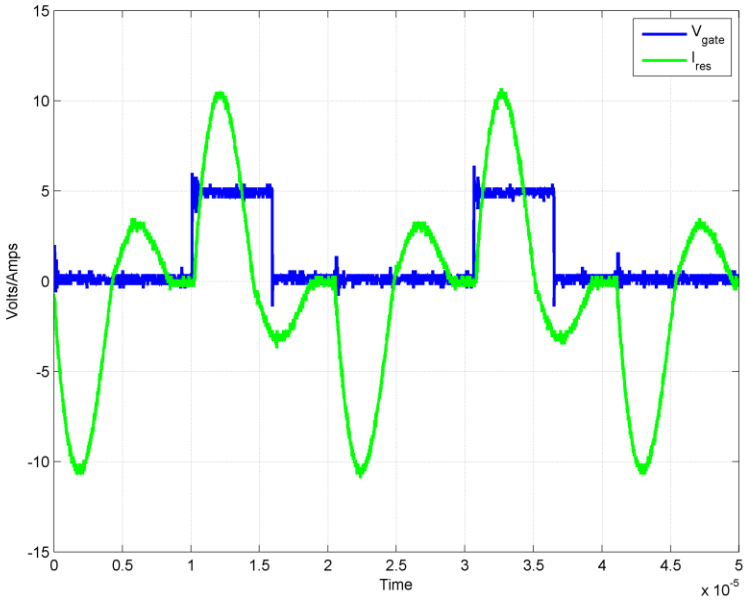


Figure 12. SLR converter waveforms using a DC power supply for the input and set at a constant switching frequency (24.7 kHz).

## C. HARDWARE TUNING

Based on the manufacturing tolerances of the components used in construction of the SLR converter, each PCB had to be tuned to ensure accuracy of the sensor measurements and the control algorithms. The process of tuning the voltage sensor to ensure accuracy of the measurements and determine the relationship between the converter output power and switching frequency necessary for proper operation of the control algorithm are detailed in the following section.

### 1. Tuning the Precision Voltage-to-Frequency Converter

The MPPT algorithm to be utilized in the PV power conditioning system required a means of sensing the PV array voltage. The output voltage of the PV array was measured using a precision voltage-to-frequency converter (LM-231) installed on the PCB. The LM-231 converter generates a square wave pulse train whose frequency is linearly mapped to the input voltage. The digital value of the input voltage is then used by the Virtex-4 FPGA to calculate the PV array output power.

Based on small variations in the circuit parameters, the LM-231 converter required tuning in order to accurately determine the PV array output voltage. The tuning of the frequency-to-voltage converter was accomplished by using the input DC power supply to vary the SLR converter input voltage (PV array output voltage) and an oscilloscope to measure the frequency of the pulse train generated by the LM-231 converter. Frequency data was collected as the input voltage was varied over the expected range of operation, 8 V to 22 V. The observed voltage and frequency data are included as Table 2. A linear least squares approximation was used to develop a best fit line for the resulting data points. The slope (gain) and *y*-intercept (offset) of the linear least squares approximation were calculated and used in the software as a gain and offset to ensure accurate output of the LM-231 converter. The experimental data and the linearized data are shown in Figure 13.

Table 2. Input voltage and frequency data.

| PV Array Output Voltage (V) | Frequency (kHz) |
|---|---|
| 8.10 | 3.60 |
| 10.16 | 4.55 |
| 12.18 | 5.44 |
| 14.23 | 6.34 |
| 16.20 | 7.15 |
| 18.20 | 8.14 |
| 20.27 | 9.00 |
| 22.23 | 9.93 |

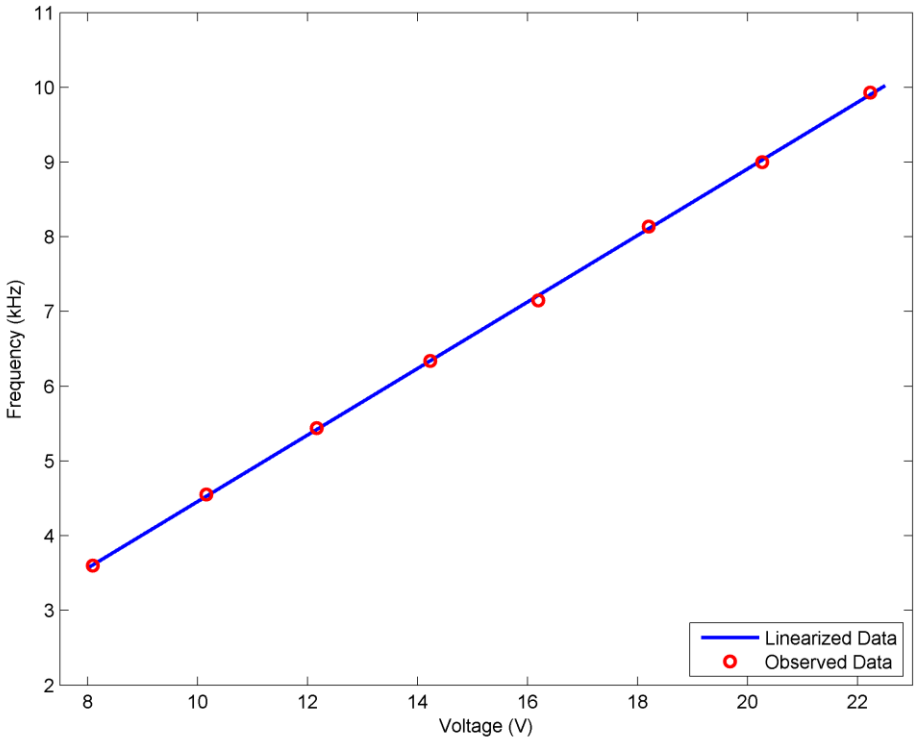


Figure 13. Plot of measured output frequency vs input voltage.

## 2. Determining the Output Current and Switching Frequency Relationship

Based on the theoretical operation of an SLR converter in DCM, it was expected that the relationship between output current and the converter switching frequency would be linear. In order to verify that the experimental relationship is linear and determine the gain and offset necessary for proper operation of the MPPT algorithm, the converter output current was measured as the switching frequency was manually varied. Using the ChipScope Pro software interface for the FPGA, we manually set the switching frequency, and the converter output current was measured. This was performed across a wide range of expected switching frequencies. This experimental data collected is provided in Table 3 and plotted in Figure 14. From Figure 14, it was observed that the current-to-frequency relationship was nearly linear as expected. The least linear squares method was applied using the data collected to determine the gain and off-set between the output current and switching frequency. These values were then used to design and simulate the MPPT algorithm.

Table 3. Load current and switching frequency measured data.

| **Switching Frequency (kHz)** | **Load Current (A)** |
|---|---|
| 41.4 | 2.74 |
| 43.9 | 2.94 |
| 46.6 | 3.28 |
| 49.8 | 3.78 |
| 53.4 | 4.08 |

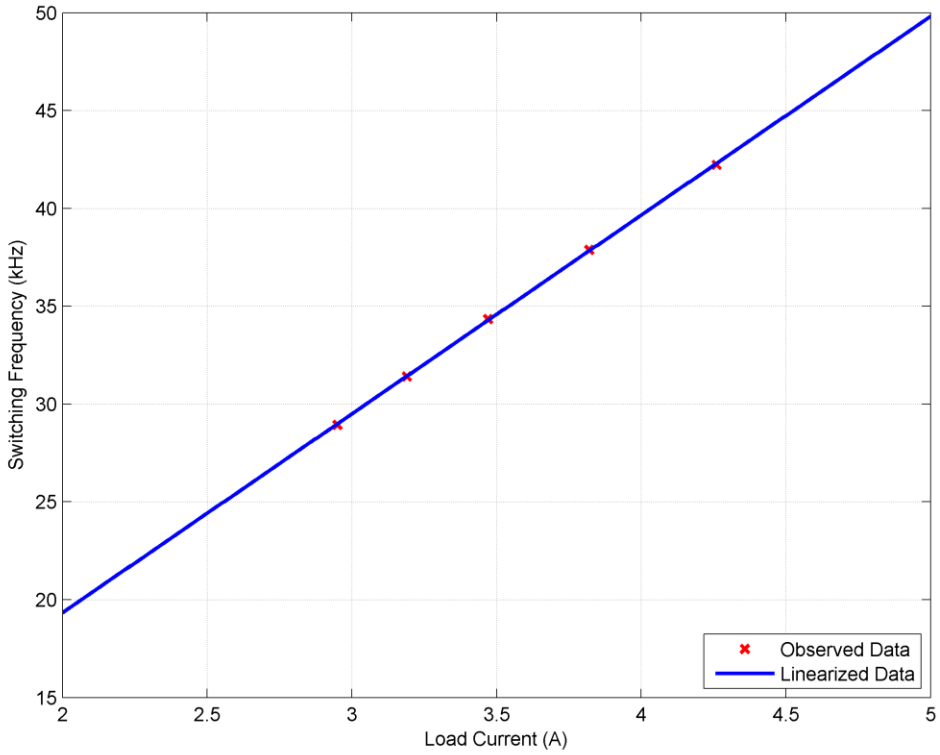


Figure 14. Plot of SLR converter switching frequency versus load current (converter output current).

# III. MODELING AND SIMULATIONS

With the observed behavior of the SLR converter known, the MPPT algorithm was simulated using both a physics-based model and a behavioral model. The process of modeling the PV array and the MPPT algorithm is detailed in the following section.

## A. PV ARRAY MODEL

In order to test the simulation of the MPPT algorithm, a PV array model was built based on the electrical representation of a PV cell as shown in Figure 15. Since the PV array model was to be implemented in Simulink, a mathematical equation that represents the operation of the PV array was first derived.

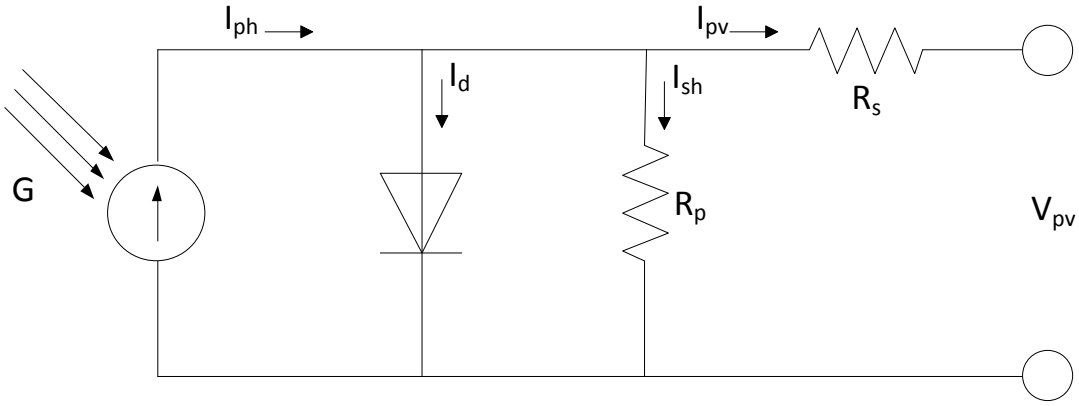


Figure 15. Electrical diagram of a PV cell.

Applying Kirchhoff's current law to the electrical diagram of the PV cell in Figure 15 produced

$$I_{pv} = I_{ph} - I_d - I_{sh}, \tag{6}$$

where $I_{pv}$ is the photovoltaic output current, $I_{ph}$ is the photocurrent, $I_d$ is the diode saturation current and $I_{sh}$ is the shunt current. For each of the three currents, $I_{ph}$, $I_d$, and, $I_{sh}$, a separate mathematical expression was developed. Equation 7 is the mathematical expression for the photocurrent of the PV cell,

$$I_{ph} = \left[ I_{sc} - K_I \left( T_c - T_{ref} \right) \right] \frac{G}{1000}, \tag{7}$$

which depends on the short-circuit current of the PV array $I_{sc}$, the temperature coefficient of the cell $K_I$, the cell temperature (in K), the cell reference temperature of 25 K, and the irradiance of the cell $G$. The mathematical expression for $I_d$ required deriving an expression for the PV cell saturation current $I_s$,

$$I_s = I_{rs} \left( \frac{T_c}{T_{ref}} \right)^3 e^{\left[ \frac{q^* E_{gap}}{\eta k} \left( \frac{1}{T_{ref}} - \frac{1}{T_c} \right) \right]}, \tag{8}$$

where $I_{rs}$ is the cell reverse saturation current, $E_{gap}$ is the band-gap energy of the semiconductor used in the cell, $\eta$ is the diode ideality factor, and $k$ is Boltzmann's constant ($1.61 \times 10^{-19}$ C). This expression was substituted into the expression for the current through a diode,

$$I_d = I_s \left[ e^{q(V_{pv} + I_{pv} R_s) / \eta k T} - 1 \right], \tag{9}$$

to produce the expression for the diode saturation current. Applying Kirchhoff's voltage law to the circuit in Figure 15 yields an equation for the shunt current $I_{sh}$,

$$I_{sh} = \frac{V_{pv} + I_{pv} R_s}{R_p}, \tag{10}$$

where $V_{pv}$ and $I_{pv}$ are the output voltage and current of the cell, respectively, and $R_s$ and $R_p$ are the series and parallel resistances associated with the cell. Finally, substituting (7), (9), and (10) into (6) produces the expression for $I_{pv}$,

$$I_{pv} = I_{ph} - I_s \left[ e^{q(V_{pv} + I_{pv} R_s) / \eta k T} - 1 \right] - \frac{V_{pv} + I_{pv} R_s}{R_p}. \tag{11}$$

Equation (11) is the basis for the mathematical expression used to build the physics-based model of a PV array in Simulink for testing of the MPPT algorithm.

The values used in the Simulink model are presented in Table 4. The values in **bold** were provided by the PV array manufacturer, while the rest of the values were either experimentally determined or assumed based on typical values used in previous research.

Table 4. Values used in simulation of PV array.

| Parameter | Symbol | Value |
|---|---|---|
| Open-Circuit Voltage | $V_{oc}$ | **21 V** |
| Short-Circuit Current | $I_{sc}$ | **2.54 A** |
| Temperature Coefficient | $K_I$ | 0.0032 |
| Reference Temperature | $T_{ref}$ | **25 C** |
| Cell Temperature | T | Variable |
| Irradiance | G | Variable |
| Electron Charge | q | $1.61x10^{-19}$ C |
| Diode Ideal Factor | η | 1.0 |
| Band-Gap Energy (c-Si) | $E_{gap}$ | 1.1 eV |
| Boltzmann's Constant | k | 1.38e-23 J/K |
| Series Resistance | $R_s$ | 0.5 Ω |
| Shunt Resistance | $R_p$ | 100 Ω |
| Cell Reverse Saturation Current | $I_{rs}$ | 1.1 A |

In the Simulink model, the PV array temperature and irradiance values are configurable as either a constant or a time-varying value to test the response of the MPPT algorithm to simulated varying environmental conditions. At the output of the PV array, Gaussian white noise was added to simulate the measurement variations that were introduced to the embedded MPPT algorithm and associated SLR converter controller.

## B. CONVERTER CONTROL AND MPPT ALGORITHM

The SLR converter presented in this thesis is digitally controlled by a Virtex-4 FPGA mounted on a developmental board. The MPPT algorithm is digitally embedded in the controller in order to optimize the power output of the PV module by scheduling the switching frequency of the SLR converter based on the linear relationship shown in Figure 14. The P&O method is the chosen MPPT algorithm and provided the base for the converter control simulations.

With the MPPT algorithm embedded in the controller, the SLR converter response to simulated varying environmental conditions was observed and was compared

to the final hardware results obtained in the laboratory. The simulated variations included PV array irradiance (shading of individual cells in the PV array) and PV array temperature. To optimize the output power of the PV array, a faster response rate is desired while minimizing the oscillations around the maximum power point during steady-state conditions. The simulation was used to determine the optimal sampling rate, switching frequency update rate, and $\Delta I$ to ensure converter stability while maximizing the converter response to fluctuating environmental conditions.

Two simulations were created to observe the proper operation the MPPT algorithm. The first simulation was a physics-based simulation built using Simulink, while the second is a behavioral model using Xilinx System Generator.

## C. PHYSICS BASED MODEL

Two variations of the P&O method MPPT algorithms were developed and simulated in Simulink, a voltage and current sensor design and the voltage sensor only design. The general block diagrams for each design are shown in Figure 16.

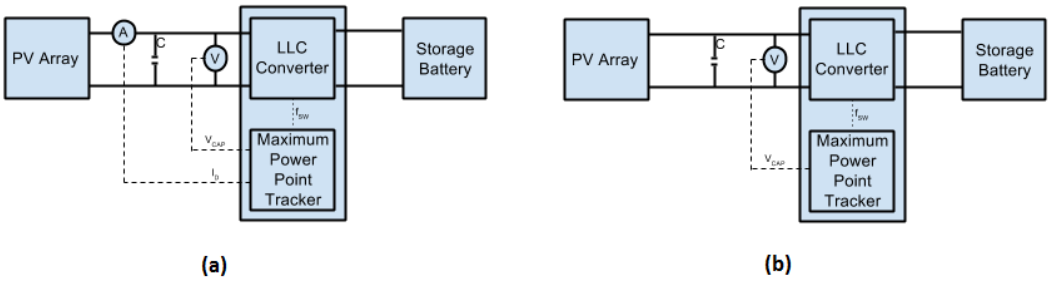


Figure 16. (a) MPPT algorithm using both voltage and current inputs. (b) MPPT algorithm using only voltage input.

### 1. Voltage and Current Sensor Design

The voltage and current sensor design MPPT algorithm utilizes the voltage sensor mounted on the PCB and an analog current sensor mounted on the Virtex-4 development board to determine the PV array output power. A software based first-order, low-pass filter with a cutoff frequency of 30 Hz was added to the model both to minimize the

effects of the noise as well as to examine the effects of the low-pass filter on the algorithm operation. The algorithm schedules the load current based on a comparison of the current output power to the previous sample output power. If the output power is increasing, the algorithm schedules more load current until the power peaks at the maximum power point. If power decreases between samples, the load current is decreased. The model of the P&O MPPT algorithm produced in Simulink is shown in Figure 17.

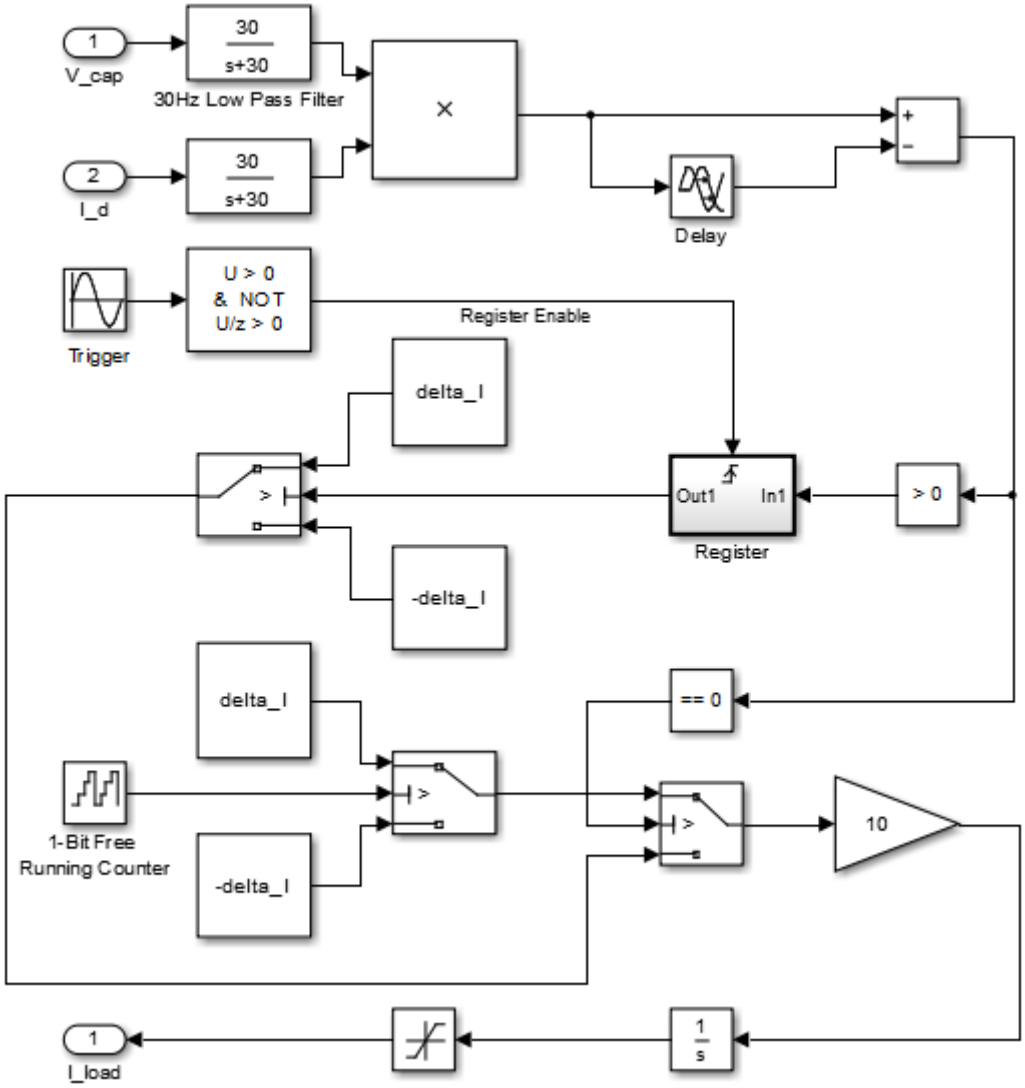


Figure 17. Block diagram of P&O MPPT algorithm in Simulink.

During the initial simulations of the MPPT algorithm, a negative bias was observed, causing the switching frequency to slowly decrease over time regardless of the PV array output power trends. The negative bias was traced back to the software based low-pass filters on the output of each sensor. When comparing the previous and current power measurements, the resultant error was frequently equal to zero when it should have been a relatively small value based on the simulated environmental conditions. This was due to the time-based averaging effect of the low-pass filter eliminating the small fluctuations in the sensor measurements driving the error to zero unless large variations in the environmental conditions were simulated. Since the MPPT algorithm needs to be able to respond to both large and small variations in environmental conditions, the Simulink model was modified. In Figure 16, the error is compared to zero, and the Boolean output dictates whether the desired current should be increased or decreased by $\Delta I$. Because the error signal was frequently equal to zero, the desired current, and, thus, the scheduled switching frequency was decreased. A second comparator block that compares the current value of output power to zero was added to the Simulink model. When the Boolean output of the second comparator block is true, a 1-bit free running counter oscillates between incrementing and decrementing the desired current. When the Boolean output is false, the perturbation is based on the value of the error signal.

The physics based model was simulated with both static and varying conditions using the simulated PV array to generate the MPPT algorithm inputs. Using the PV array model from the previous section, we simulated multiple voltage versus current profile curves using different values of irradiance. The simulated PV array response to increasing $G$ using the MPPT algorithm was then superimposed over these profile curves to demonstrate that operation of the MPPT algorithm. From Figure 18, it is observed that the MPPT algorithm is forcing the simulated PV array output to operate at the maximum power point.

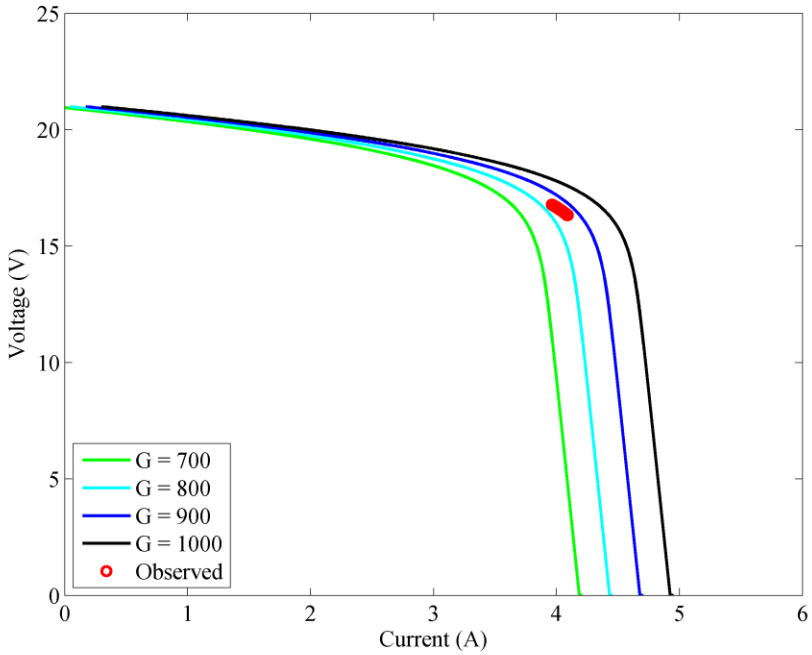


Figure 18. Simulated PV array response to an increase in *G* plotted as voltage versus current.

From Figure 19, the same response is seen plotted as power versus current. The trajectory of the PV array operating point (shown as observed data in Figures 18 and 19) indicates that the MPPT algorithm is forcing the PV array output towards the maximum power point as *G* is increased. The oscillations about the maximum power point as described in the previous subsection of this thesis can be seen in Figures 18 and 19. From these simulations, $\Delta I$ was set to 1 mA as this value provided a good balance between a fast MPPT algorithm response while minimizing the PV array output oscillations.

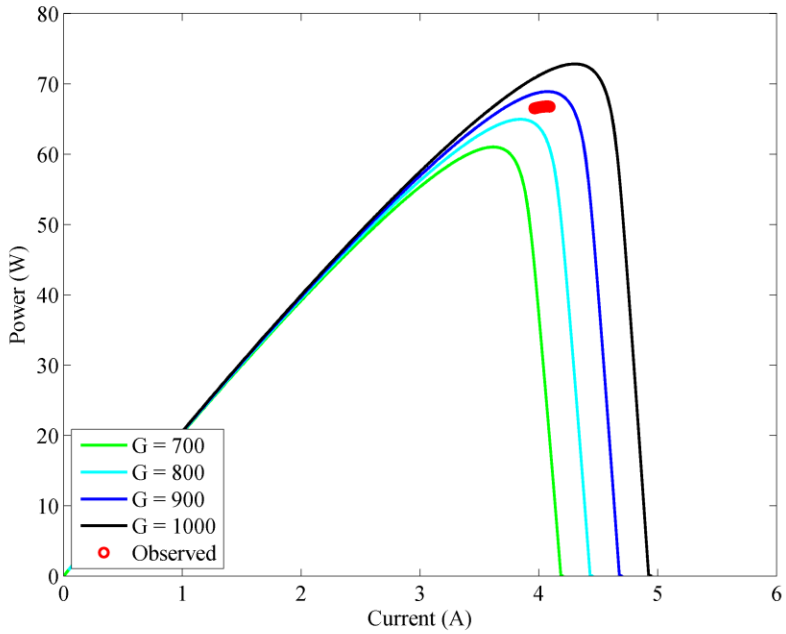


Figure 19. Simulated PV array response to an increase in *G* plotted as power versus current.

### 2. Voltage Sensor Only Design

Because the switching frequency is scheduled by the MPPT algorithm and the relationship between load current and switching frequency is known, the output current of the PV array does not have to be measured directly, eliminating the need for the current sensor. Instead, the PV output current can be estimated using switching frequency as an observer for current. This reduces the overall cost and complexity of the power conditioner as well as reducing the induced noise in the system. By scheduling the switching frequency, the algorithm estimates the load current based on the observed linear relationship and determines an estimate of the PV array output power.

The Simulink model looks identical to the model shown in Figure 17 except the PV array output current signal $I_d$ does not originate at the current sensor on the Virtex-4 development board. Instead, the signal is generated based on the linear mapping between the known scheduled switching frequency and the expected PV array output current. Because the current sensor is not utilized, the second low pass filter is not required.

An issue observed with using a current observer vice actual current measurement was that the output current of the PV array was estimated using the scheduled switching frequency. The switching frequency is linearly proportional to the load current, which is an algebraic sum of both the PV array output current and capacitor current. By using the current observer, we neglect the effects of the capacitor current, which causes errors in the simulation. To reduce the error, the sampling rate of the PV array was reduced to 10 Hz. This resulted in an average capacitor current on the order of approximately 20 mA. This relatively small value of capacitor current can be neglected when compared to the load current of approximately 4 A.

Because the Virtex-4 FPGA development board used for this experiment did have an analog current sensor available, two models were built to compare the performance of the MPPT algorithm using the current sensor and the current observer once implemented in hardware.

## D. BEHAVIORAL MODEL

The second simulation is a behavioral model of the MPPT algorithm using Xilinx System Generator software package and the ISE Design Suite. The Xilinx System Generator software utilizes a MATLAB Simulink toolbox to graphically build the MPPT algorithm in Simulink. Once the algorithm was built using the Xilinx toolbox, it was compiled in System Generator. System Generator is a high level simulation compiler that produces VHSIC hardware description language (VHDL) code for the model built in Simulink. With the VHDL code, the Xilinx ISE Design Suite software package produces the assembly code that is flashed into the Virtex-4 FPGA via the ChipScope Interface software.

The two largest differences between the Simulink model and the model designed using the Xilinx toolbox and System Generator are that the programmer must specify the precision of the fixed point numbers for mathematical operations in System Generator. This allows the programmer to allocate the appropriate amount of memory balancing the required precision of the number and limited amount of memory available on the Virtex-4 developmental board, whereas in Simulink, limitations in memory are generally not

applicable based on the abundant resources of a personal computer. From Figure 20, the fixed point notation for each value can be seen. The *ufix* designation indicates that the value is an unsigned fixed point number, while *fix* indicates a signed fixed point number (2s complement). The second difference is the coordination of sequential operations. In System Generator, each operation requires a certain number of clock cycles to be performed and must be organized such that all necessary calculations occur within a single sample period to prevent erroneous values from being passed. Delays and registers were used in the Xilinx model to prevent erroneous results from being passed to the next operation. In Figure 20, the delays utilize a *z*-transform notation to indicate the number of clock cycles the result is delayed.

The red and blue inputs in Figure 20 represent the PV array output current and voltage measurements, respectively. The green output is the scheduled switching frequency of the converter. Similar to the physics based model, the behavioral model can utilize either the voltage and current sensor design or voltage sensor only design in the implementation of the MPPT algorithm with the only difference being whether $I_d$ is a direct measurement from the analog current sensor or estimated based on the scheduled switching frequency.

As part of the current-to-frequency conversion, the reciprocal of the scheduled switching frequency is required to determine the appropriate period $T_{sw}$:

$$T_{sw} = \frac{1}{f_{sw}}. \tag{12}$$

The process of computing a fixed-point reciprocal is too computationally intensive for the Virtex-4 FPGA and required the use of a look-up table (LUT). The LUT is generated when System Generator compiles the initial conditions file associated with the behavioral model by specifying the range of possible inputs (establishing the depth of the LUT) and the corresponding result for each address value. The programmer must then define the fixed-point precision of the results (establishing the width of the LUT). The concept of LUT width and depth are illustrated in Figure 21.

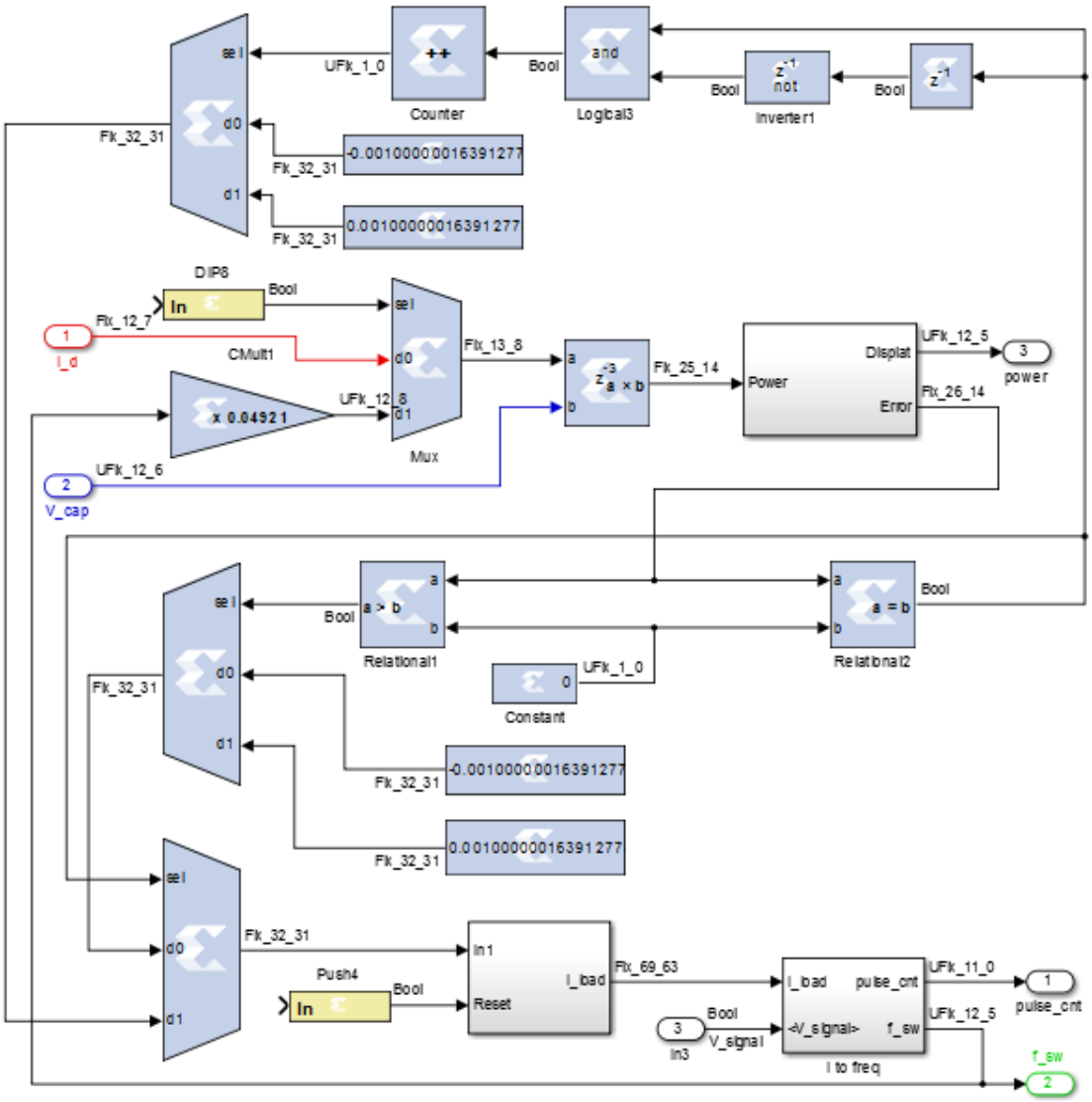


Figure 20. Block diagram of P&O MPPT algorithm in Xilinx System Generator.

The LUT is generated in the host computer where the computational resources, namely the processor and memory, are abundant and then pushed to the FPGA as machine code where it is stored in the developmental board block ROM. Using the input to the LUT as the address, the algorithm refers to the appropriate location in block ROM and returns the output of the LUT using the fixed-point precision specified by the programmer without any computations performed by the FPGA. While the use of a LUT is generally more efficient because complex mathematical operations are performed

outside of the FPGA, it does have a significant drawback. Specifically, large LUTs require a significant amount of read-only memory (ROM) as the entire range of inputs and the respective results are stored in memory. As seen in Appendix B, the Virtex-4 FPGA block ROM is limited to 1296 Kb. This limitation required that the depth and/or width of the LUT be reduced. The depth of the LUT was established based on the range of all possible inputs and, therefore, could not be reduced, so the width of the LUT was reduced such that the fixed-point precision of the output decreased from $2^{-32}$ to $2^{-15}$. This significant reduction in fixed-point number precision caused the behavioral model to be less responsive when compared to the physics based model because smaller changes in switching frequency were neglected. Reducing the output fixed-point precision had a similar effect to quantization error in an analog-to-digital converter in that small changes in the input had little or no effect on the output. This was not observed in the physics based model, where double precision floating-point numbers were used in the mathematical operations of the algorithm.

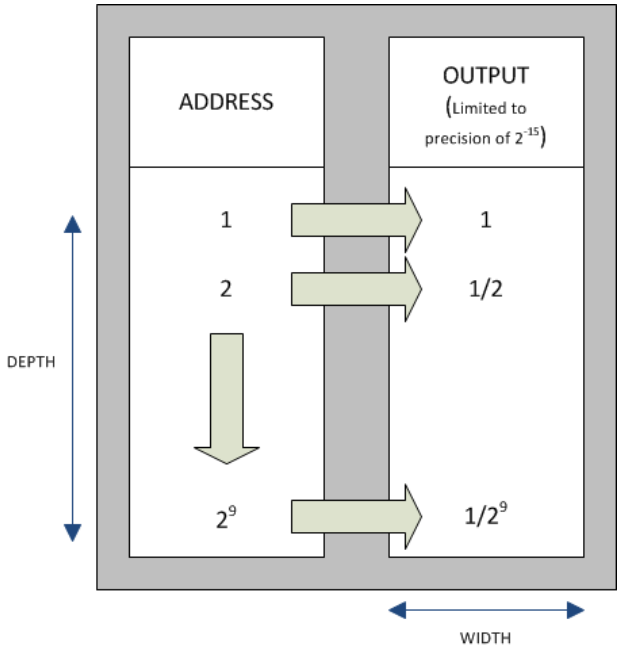


Figure 21. Diagram of a look-up table in System Generator.

The scheduling of the switching frequency must be controlled such that the switching frequency is not changed while a MOSFET gate signal is high or in the middle

of a resonant cycle. This required the use of an S-R flip-flop combined with a logical AND block to drive an enable signal for the register. A counter was used to generate a 10 Hz square wave pulse. The square wave pulse set the S-R flip-flop, whose output was then one of two inputs of a logical AND block. The other input to the logical AND block was a Boolean output signal generated based on the presence of a MOSFET gate signal. When the upper MOSFET gate went high, a Boolean true was sent to the second input on the logical AND block. When both inputs of the logical AND block were high, the Boolean output triggered an enable for a register that stored the new scheduled switching frequency. The Boolean trigger is shown as the *V_signal* in Figure 20. This forced the switching frequency to only be changed at the beginning of a resonant cycle to prevent any hard-switching of the SLR converter.

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# IV. FINAL HARDWARE TESTING AND RESULTS

Once the linear characteristics of the SLR converter were known, a 40-W PV array with an open-circuit DC output voltage of 21V and short-circuit current of 2.54 A replaced the input DC power supply used in the initial hardware test. With the PV array connected to the SLR converter, it was necessary to use a capacitor in parallel with the PV array $C_{cap}$ to minimize the PV array output voltage fluctuation caused by the converter switching events. In Figure 22, the block diagram of the setup used in the final testing of the SLR converter and MPPT algorithm can be seen.

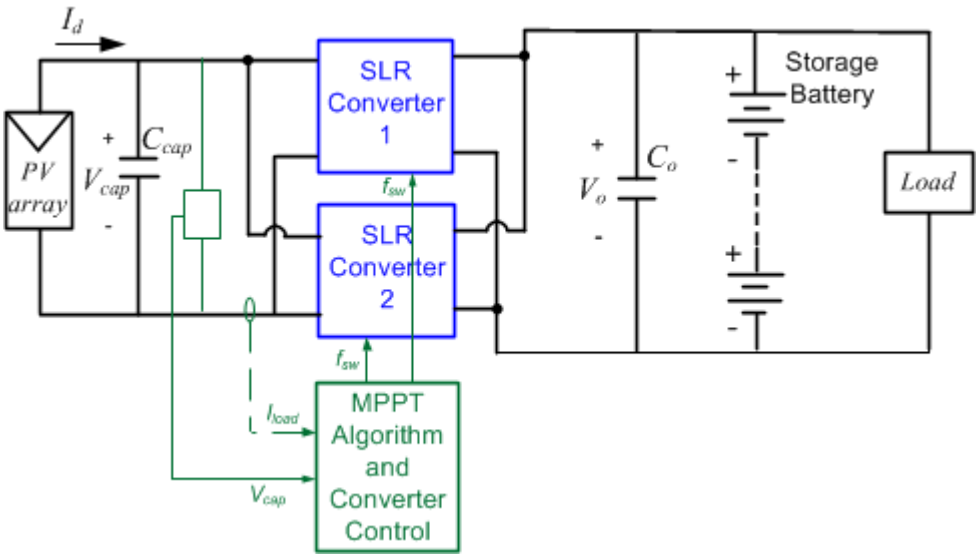



Figure 22. Block diagram of laboratory setup for final operational test.

After the preliminary testing of both the SLR converters in the laboratory and successful simulation of the MPPT algorithm in Xilinx System Generator, the MPPT algorithm and switching frequency control strategy was flashed into the Virtex-4 FPGA using the ChipScope Pro Interface. A DC power supply was connected to the output of the SLR converter to simulate a 72 V lead-acid storage battery. With the MPPT algorithm enabled using a DIP switch mounted on the Virtex-4 developmental board, observations of the switching frequency versus displayed PV array output power were made. Because of the cloud cover in Monterey, California, a single 40-W PV array did not provide

sufficient output current to overcome the losses associated with the converter. An additional 40W PV array was installed in parallel with the first to double the output current. The two SLR converters were also connected in parallel to observe the operation of the converters while connected to a single source and providing power to a single load. With the ChipScope Analyzer software, raw data output from the Virtex-4 FPGA was stored and displayed in MATLAB. Based on the limited memory available for data storage, the data was collected in 21 s intervals.

In Figure 23, the SLR converter waveforms observed during the final operational testing can be observed. The gate voltage signal and resonant voltage and resonant current data shown was collected from a single SLR converter, while the output current $I_{out}$ was the combined output current from both SLR converters. The combined output current did have a significant amount of ripple; however, this could have been reduced by interleaving the gate voltage signals between the two SLR converters. Because the gate signal is common to both SLR converters, the resonant current pulses occurred simultaneously. If the gate signals were staggered between the SLR converters such that the resonant current peaks were offset, the ripple would have been reduced.

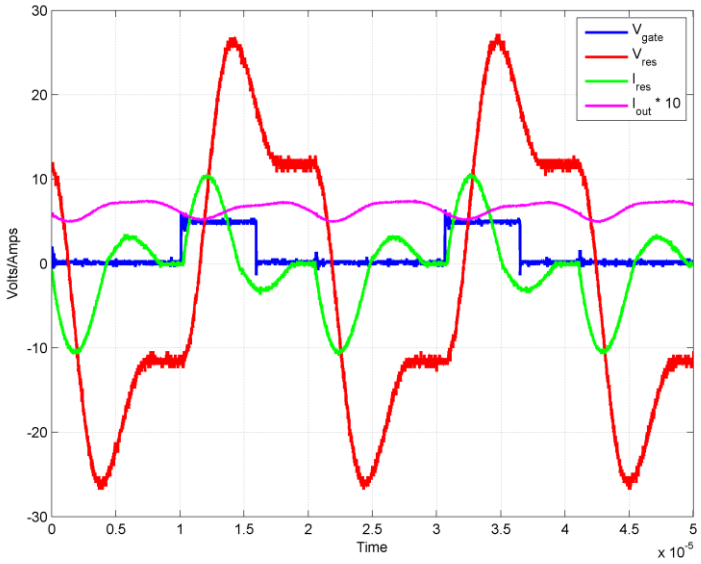



Figure 23. Observed SLR converter waveforms observed during final laboratory testing.

From Figure 24 and Figure 25, the response to a slow increase in irradiance can be seen for both the voltage and current sensor MPPT algorithm design and the voltage sensor only MPPT algorithm design, respectively. This was accomplished by slowly rotating the PV arrays toward the sun over a 20 s period.

Comparing the response of each MPPT algorithm design, we noted that the response of the voltage sensor only design was slower than that of the voltage and current sensor. This is attributed to the reduced sampling frequency of the PV array output parameters. As the irradiance of the PV array increases, the maximum power point of the PV array also increases. The observed response is that the MPPT algorithm increases the scheduled switching frequency of the converter and, in turn, causes the output current to increase. The decrease in voltage is the non-linear voltage sag that occurs as the PV array current increases (see Figure 5).

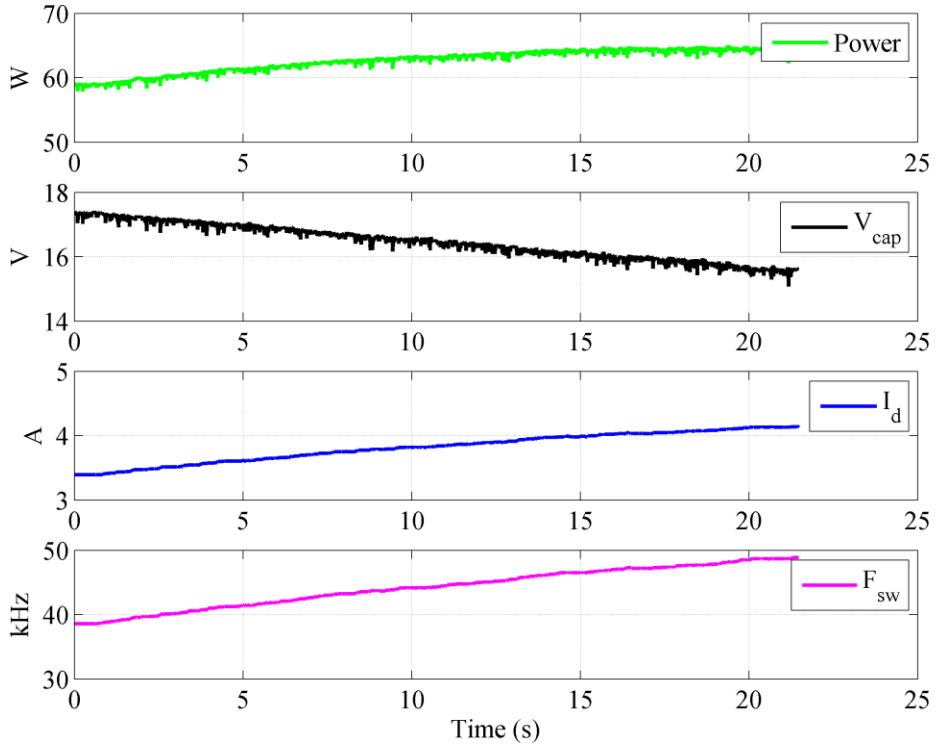



Figure 24. SLR converter waveforms when slowly increasing the PV array irradiance using the voltage and current sensor MPPT design.

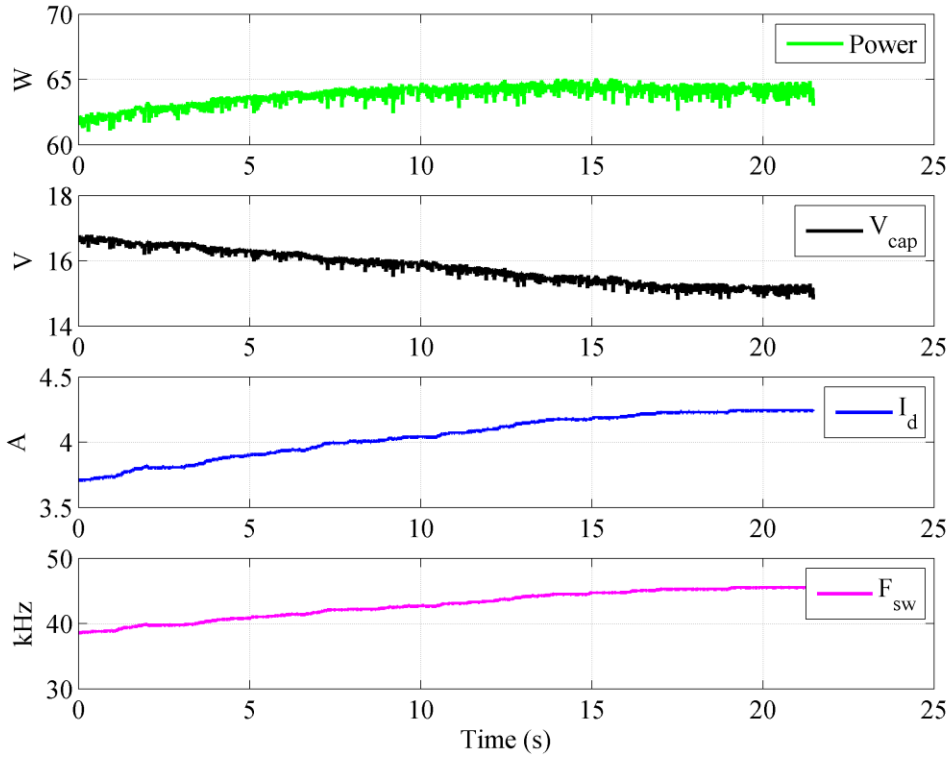



Figure 25. SLR converter waveforms when slowly increasing the PV array irradiance using the voltage sensor only MPPT design.

From Figure 26 and Figure 27, the response to a step decrease in irradiance can be seen for both the voltage and current sensor MPPT algorithm design and the voltage sensor only MPPT algorithm design, respectively. This was accomplished by rotating the PV arrays away from the sun over a 5 s period. As was observed in the previous figures, when the irradiance of the PV array is decreased, the switching frequency is lowered until a new steady-state maximum power point is reached for the new environmental conditions. The increase in switching frequency observed near the end of Figure 26 was based on an operator error during the test.

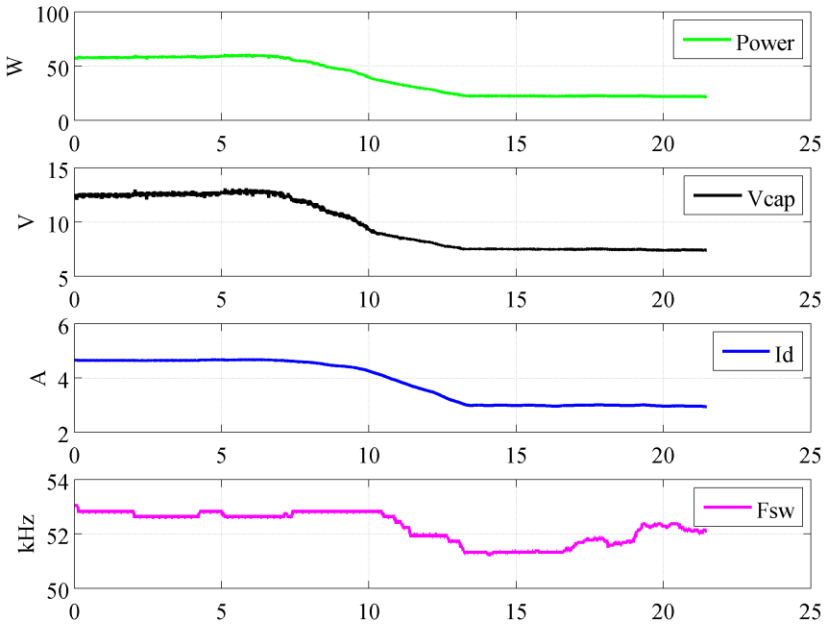



Figure 26. SLR converter waveforms based on a step decrease of the PV array irradiance using the voltage and current sensor MPPT algorithm design.

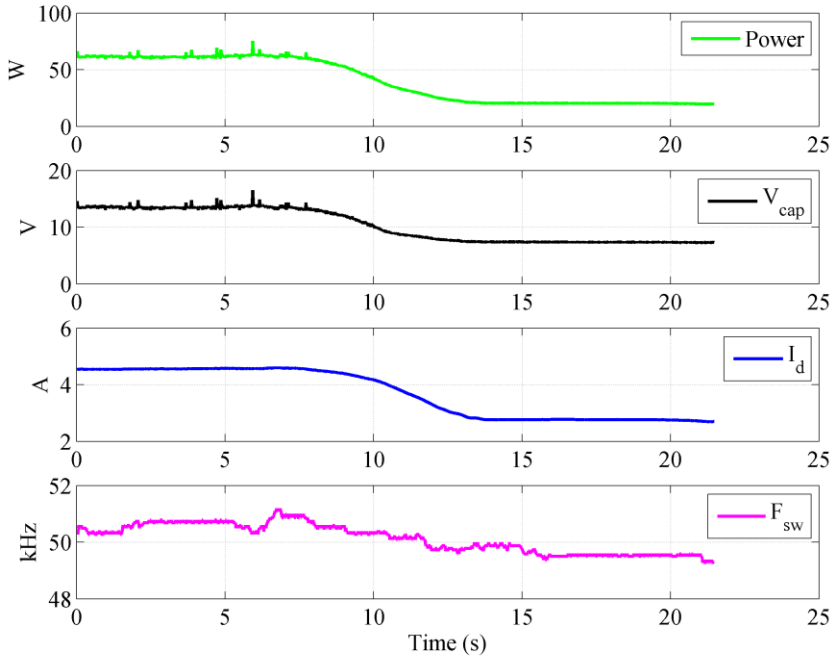



Figure 27. SLR converter waveforms based on a step decrease of the PV array irradiance using the voltage sensor only MPPT algorithm design.

From Figures 24 through 27, we see that the MPPT algorithm tracks the optimal operating point while the environmental conditions vary. The MPPT algorithm tracks the optimal operating point through slow variations in environmental conditions as well as quickly changing conditions.

Typical voltage versus current profile curves were generated for multiple irradiance values using the PV array model described in the previous section. The effects of variations in PV array temperature were neglected for these simulations. From Figure 28, it can be seen that the MPPT algorithm forces the PV array to operate at the maximum power point when the observed PV array output is superimposed over the simulated PV array voltage versus current curves. From Figure 29, the same observed PV array output response is plotted as power versus current and superimposed on the typical power versus current profile curves produced at multiple irradiance values. The proper operation of the MPPT algorithm is demonstrated by Figures 28 and 29.

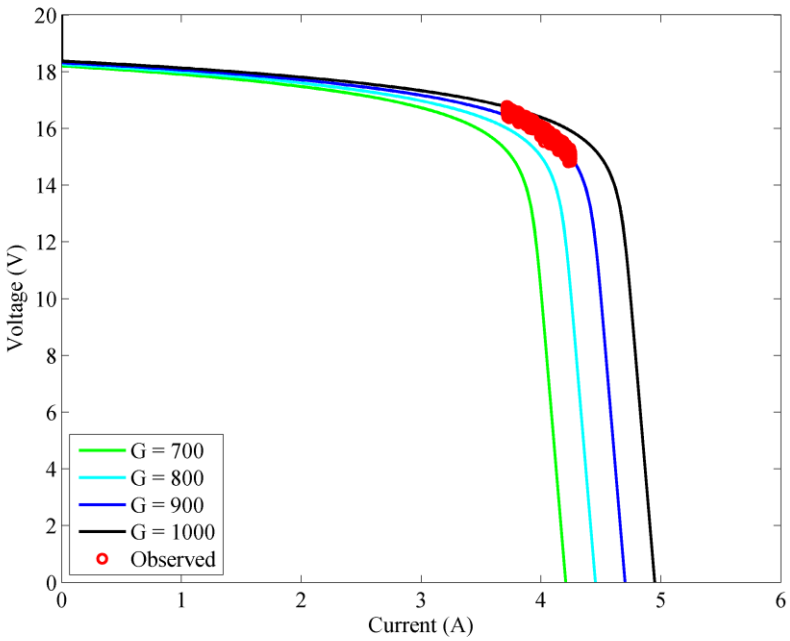



Figure 28. PV array output superimposed over simulated PV array voltage versus current curves at various irradiance values *G*.

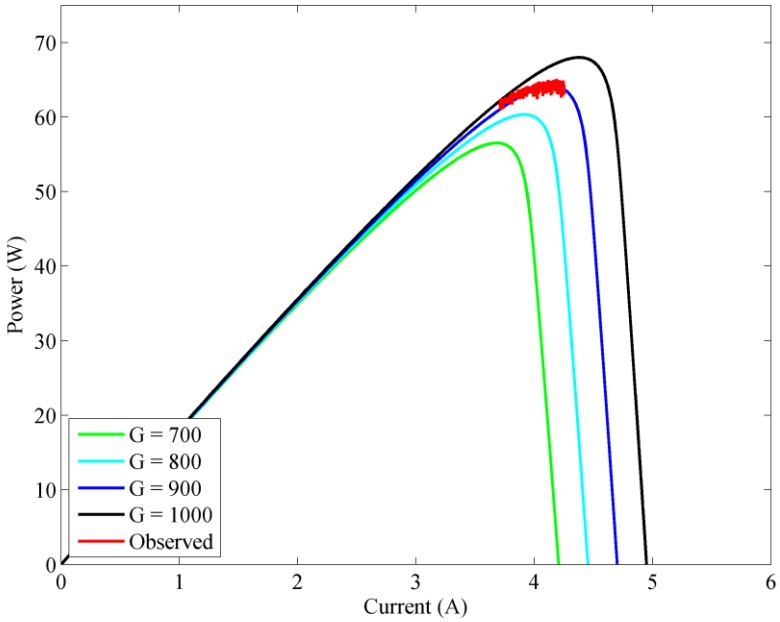



Figure 29. PV array output superimposed over simulated PV array power versus current curves at various irradiance values *G*.

Input and output power data was collected during operation of the SLR converter to analyze the efficiency at varying switching frequencies. The overall efficiency of the SLR converter varied between 55 percent and 60 percent and was based on the switching frequency. The power and efficiency data was tabulated and is provided in Table 5. These efficiency values were compared to the SLR converter efficiency achieved in [18] as a means of determining if the losses associated with the SLR converter design used in this research were consistent with the losses in other SLR converter designs.

Table 5. Input and output power data.

| **Switching Frequency (kHz)** | **Input Power (W)** | **Output Power (W)** | **Efficiency (%)** |
|---|---|---|---|
| 41.40 | 38.36 | 23.03 | 60.0 |
| 43.90 | 41.16 | 23.15 | 56.2 |
| 46.60 | 45.92 | 25.71 | 55.9 |
| 49.80 | 52.92 | 29.64 | 56.0 |
| 53.40 | 57.12 | 31.64 | 55.4 |

These efficiency values were consistent for an SLR converter operating in DCM based on data presented in Table 5. Had the SLR converter been operated in CCM, the efficiencies would have been higher based on having higher resonant tank impedance. The higher resonant impedance reduces the peak of the resonant current pulses and results in smaller conduction losses. Another concern related to operation in DCM vice CCM is the shape of the resonant current waveform. Of the three modes of operation, DCM yields the most distorted current waveform indicating more harmonics in the waveform compared to the waveform produced in the other two modes of operation. With more harmonics the circuit has higher conduction and core losses.

# V. CONCLUSION AND FUTURE WORK

The research presented in this thesis indicates that the application of the SLR converter setup shown in this thesis is an attractive DC-DC converter topology to interface a PV module to an existing DC bus. An SLR converter in DCM behaves very much like a current source, which makes parallel operation simple. In addition, the digitally embedded MPPT algorithm increases the efficiency of the system by ensuring that the PV array output is optimized for the current environmental conditions. The combination of the PV array operating point optimization and the higher efficiencies observed with the SLR converter show that this topology is an ideal application for the solar industry.

The linear operation of the SLR converter allows multiple SLR converters to be connected in parallel to support higher power applications. This capability is significant as there is an increased interest in having small power converters for each PV cell vice a large central power converter for the entire PV array as a means to improve the overall system efficiency [15]. Using an SLR converter with an embedded MPPT algorithm at the output of each cell allows each cell operate at the maximum power point independent of the array, increasing the output power of the PV array. A DC-DC converter topology that can be implemented in a PV array interface application that requires multiple converters because, as ideal current sources, SLR converters readily accept being paralleled was investigated in this thesis.

## A. FUTURE WORK

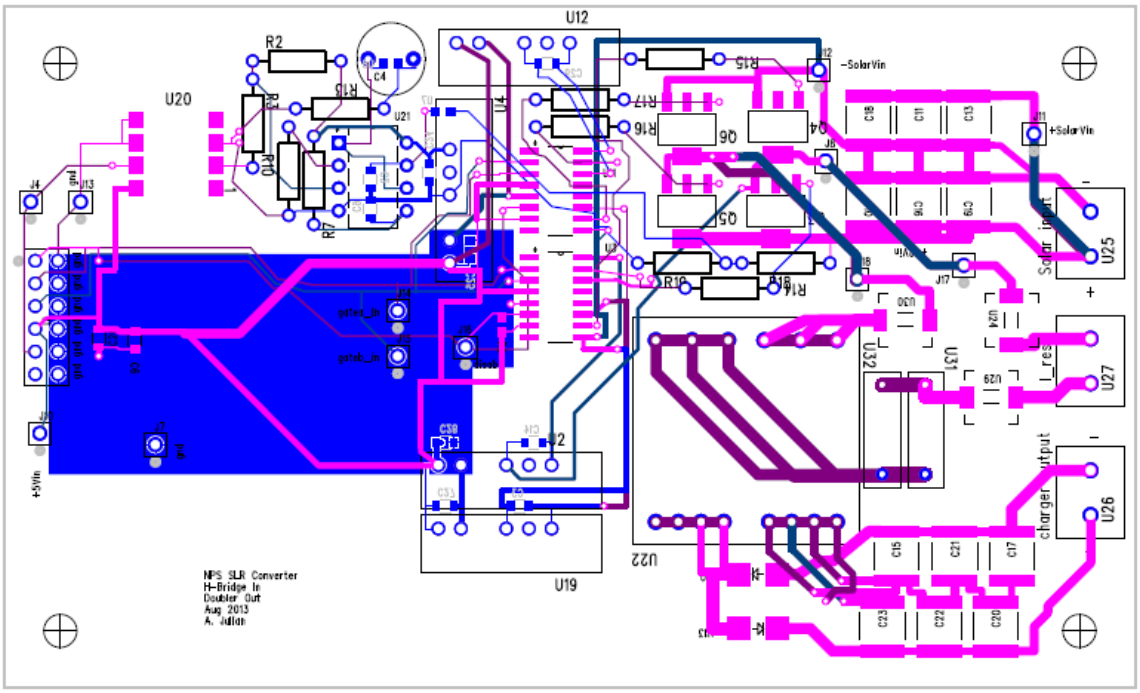
The efficiency of the SLR converter was consistent with the efficiency achieved in [18] but could be improved with a better design and higher quality components. Future work related to this topic could include correcting the sources of heat loss identified in the SLR converter design used:

- High conduction losses in the transformer windings due to the high switching frequency (effects of skin depth) and the small diameter windings used in construction of the transformer.

- Poor heat removal from the MOSFETs. The MOSFET manufacturer recommended a 1 in by 1 in copper heat sink at each mounting location. The PCB design did not include the necessary footprint to accommodate the recommended heat sink. Instead, forced air circulation was utilized.
- High conduction loss in the MOSFETs due to the relatively large $R_{ds}$.

Another related topic is to examine the advantage of operating the SLR converter in CCM in a PV application. Operation of the SLR converter in DCM was chosen because the ideal current source behavior was attractive as an interface between a PV array and micro-grid; however, efficiency data provided in [18] indicates that higher efficiencies are achievable in CCM. The higher efficiency of the SLR converter operating in CCM may be a more attractive feature compared to the fine power flow control and, thus, be the more attractive converter topology for a PV application.

# APPENDIX A. PRINTED CIRCUIT BOARD LAYOUT OF SLR CONVERTER



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# APPENDIX B. VIRTEX-4 FIELD PROGRAMMABLE GATE ARRAY DATA SHEET

XILINX®

## Virtex-4 Family Overview

DS112 (v3.1) August 30, 2010 **Product Specification**

### General Description

Combining Advanced Silicon Modular Block (ASMBL™) architecture with a wide variety of flexible features, the Virtex®-4 family from Xilinx greatly enhances programmable logic design capabilities, making it a powerful alternative to ASIC technology. Virtex-4 FPGAs comprise three platform families—LX, FX, and SX—offering multiple feature choices and combinations to address all complex applications. The wide array of Virtex-4 FPGA hard-IP core blocks includes the PowerPC® processors (with a new APU interface), tri-mode Ethernet MACs, 622 Mb/s to 6.5 Gb/s serial transceivers, dedicated DSP slices, high-speed clock management circuitry, and source-synchronous interface blocks. The basic Virtex-4 FPGA building blocks are enhancements of those found in the popular Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X product families, so previous-generation designs are upward compatible. Virtex-4 devices are produced on a state-of-the-art 90 nm copper process using 300 mm (12-inch) wafer technology.

### Summary of Virtex-4 Family Features

- Three Families — LX/SX/FX
  - Virtex-4 LX: High-performance logic applications solution
  - Virtex-4 SX: High-performance solution for digital signal processing (DSP) applications
  - Virtex-4 FX: High-performance, full-featured solution for embedded platform applications
- Xesium™ Clock Technology
  - Digital clock manager (DCM) blocks
  - Additional phase-matched clock dividers (PMCD)
  - Differential global clocks
- XtremeDSP™ Slice
  - 18 x 18, two's complement, signed Multiplier
  - Optional pipeline stages
  - Built-in Accumulator (48-bit) and Adder/Subtracter
- Smart RAM Memory Hierarchy
  - Distributed RAM
  - Dual-port 18-Kbit RAM blocks
    - Optional pipeline stages
    - Optional programmable FIFO logic automatically remaps RAM signals as FIFO signals
  - High-speed memory interface supports DDR and DDR-2 SDRAM, QDR-II, and RLDRAM-II.
- SelectIO™ Technology
  - 1.5V to 3.3V I/O operation
  - Built-in ChipSync™ source-synchronous technology
  - Digitally controlled impedance (DCI) active termination
  - Fine grained I/O banking (configuration in one bank)
- Flexible Logic Resources
- Secure Chip AES Bitstream Encryption
- 90 nm Copper CMOS Process
- 1.2V Core Voltage
- Flip-Chip Packaging including Pb-Free Package Choices
- RocketIO™ 622 Mb/s to 6.5 Gb/s Multi-Gigabit Transceiver (MGT) [*FX only*]
- IBM PowerPC RISC Processor Core [*FX only*]
  - PowerPC 405 (PPC405) Core
  - Auxiliary Processor Unit Interface (User Coprocessor)
- Multiple Tri-Mode Ethernet MACs [*FX only*]

*Table 1:* **Virtex-4 FPGA Family Members**

| Device | Configurable Logic Blocks (CLBs)[1] | | | | XtremeDSP Slices[2] | Block RAM | | DCMs | PMCDs | PowerPC Processor Blocks | Ethernet MACs | RocketIO Transceiver Blocks | Total I/O Banks | Max User I/O |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Array[3] Row x Col | Logic Cells | Slices | Max Distributed RAM (Kb) | | 18 Kb Blocks | Max Block RAM (Kb) | | | | | | | |
| XC4VLX15 | 64 x 24 | 13,824 | 6,144 | 96 | 32 | 48 | 864 | 4 | 0 | N/A | N/A | N/A | 9 | 320 |
| XC4VLX25 | 96 x 28 | 24,192 | 10,752 | 168 | 48 | 72 | 1,296 | 8 | 4 | N/A | N/A | N/A | 11 | 448 |
| XC4VLX40 | 128 x 36 | 41,472 | 18,432 | 288 | 64 | 96 | 1,728 | 8 | 4 | N/A | N/A | N/A | 13 | 640 |
| XC4VLX60 | 128 x 52 | 59,904 | 26,624 | 416 | 64 | 160 | 2,880 | 8 | 4 | N/A | N/A | N/A | 13 | 640 |
| XC4VLX80 | 160 x 56 | 80,640 | 35,840 | 560 | 80 | 200 | 3,600 | 12 | 8 | N/A | N/A | N/A | 15 | 768 |
| XC4VLX100 | 192 x 64 | 110,592 | 49,152 | 768 | 96 | 240 | 4,320 | 12 | 8 | N/A | N/A | N/A | 17 | 960 |
| XC4VLX160 | 192 x 88 | 152,064 | 67,584 | 1056 | 96 | 288 | 5,184 | 12 | 8 | N/A | N/A | N/A | 17 | 960 |
| XC4VLX200 | 192 x 116 | 200,448 | 89,088 | 1392 | 96 | 336 | 6,048 | 12 | 8 | N/A | N/A | N/A | 17 | 960 |

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